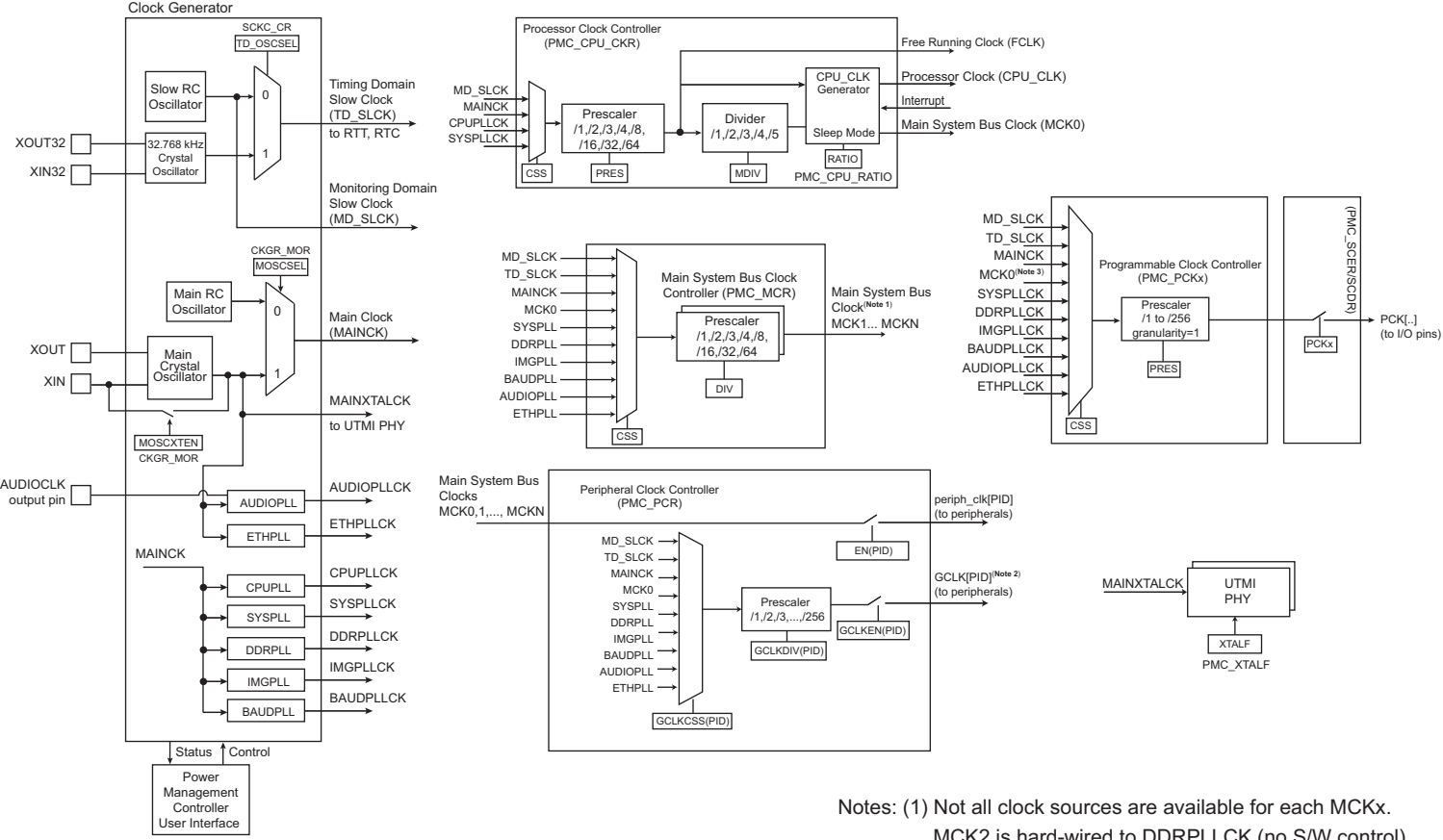

Notes: (1) Not all clock sources are available for each MCKx.
MCK2 is hard-wired to DDRPLLCK (no S/W control).
(2) Not all clock sources are available for each GCLK[PID].
(3) As MCK0=CPU_CLK/PMC_CPU_CKR.MDIV,
MCK0 is not independent from CPU_CLK. Take this into account in case of CPU frequency scaling.