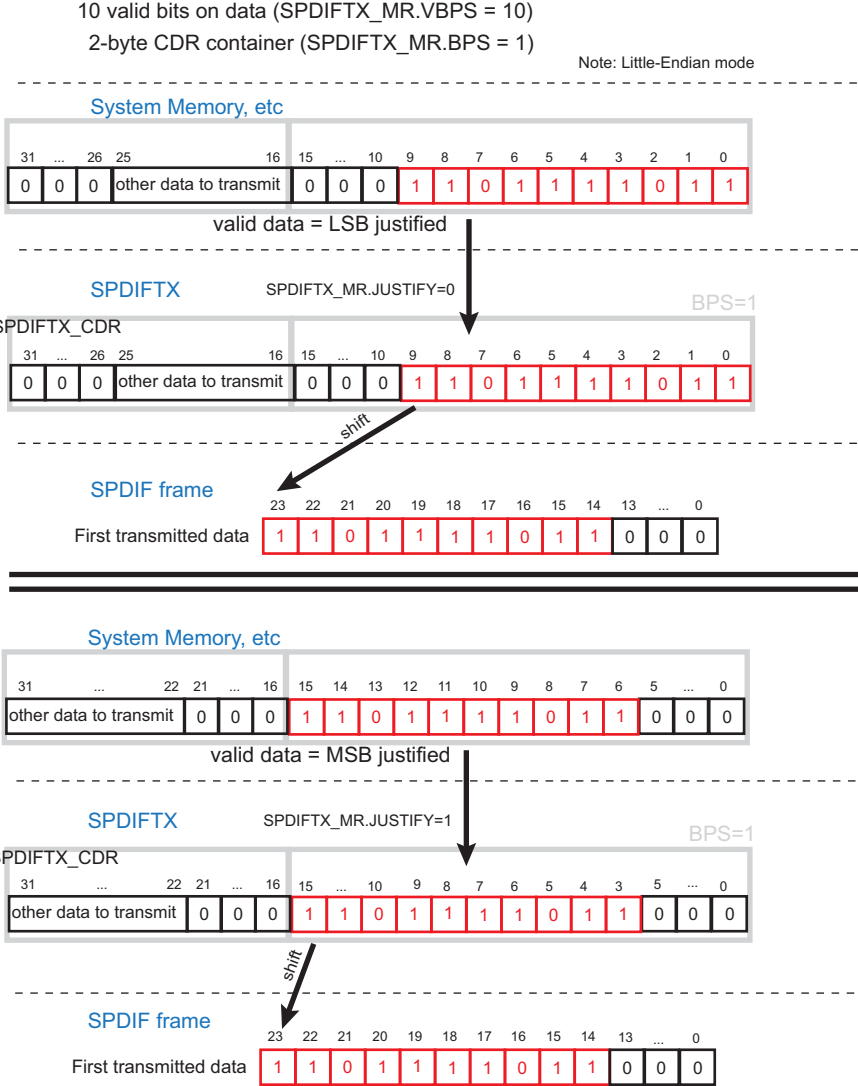
10 valid bits on data (SPDIFTX_MR.VBPS = 10)
2-byte CDR container (SPDIFTX_MR.BPS = 1)
Note: Little-Endian mode
System Memory, etc
31 ... 26 25 16 15 ... 10 9 8 7 6 5 4 3 2 1 0
0 0 0 other data to transmit 0 0 0 1 1 0 1 1 1 1 0 1 1
valid data = LSB justified
SPDIFTX
SPDIFTX_MR.JUSTIFY=0
BPS=1
SPDIFTX_CDR
31 ... 26 25 16 15 ... 10 9 8 7 6 5 4 3 2 1 0
0 0 0 other data to transmit 0 0 0 1 1 0 1 1 1 1 0 1 1
shift
SPDIF frame
23 22 21 20 19 18 17 16 15 14 13 ... 0
First transmitted data
1 1 0 1 1 1 1 0 1 1 0 0 0
System Memory, etc
31 ... 22 21 ... 16 15 14 13 12 11 10 9 8 7 6 5 ... 0
other data to transmit 0 0 0 1 1 0 1 1 1 1 0 1 1 0 0 0
valid data = MSB justified
SPDIFTX
SPDIFTX_MR.JUSTIFY=1
BPS=1
SPDIFTX_CDR
31 ... 22 21 ... 16 15 ... 10 9 8 7 6 5 4 3 5 ... 0
other data to transmit 0 0 0 1 1 0 1 1 1 1 0 1 1 0 0 0
shift
SPDIF frame
23 22 21 20 19 18 17 16 15 14 13 ... 0
First transmitted data
1 1 0 1 1 1 1 0 1 1 0 0 0