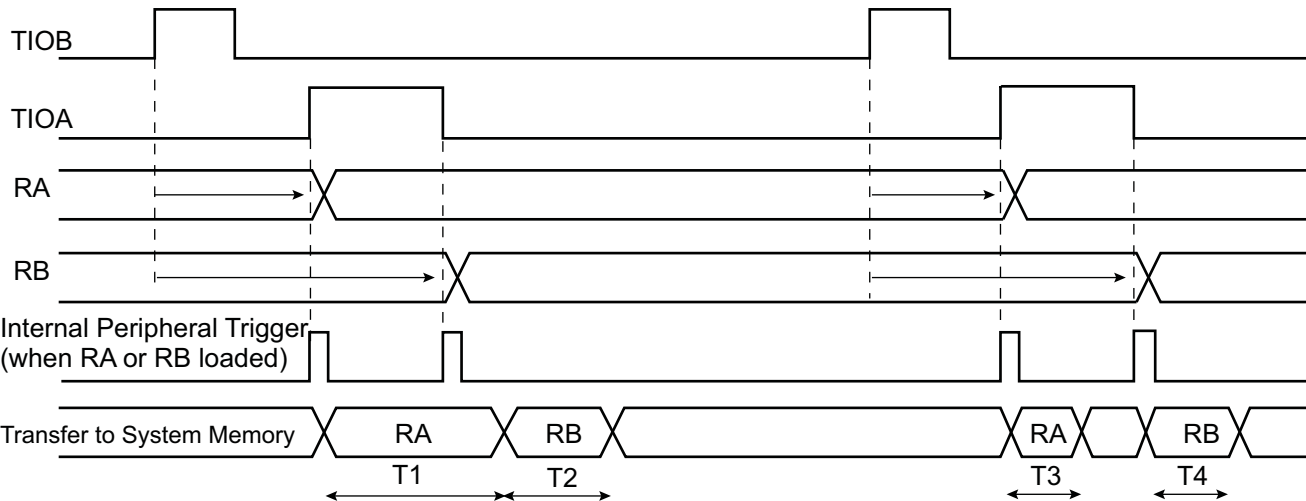
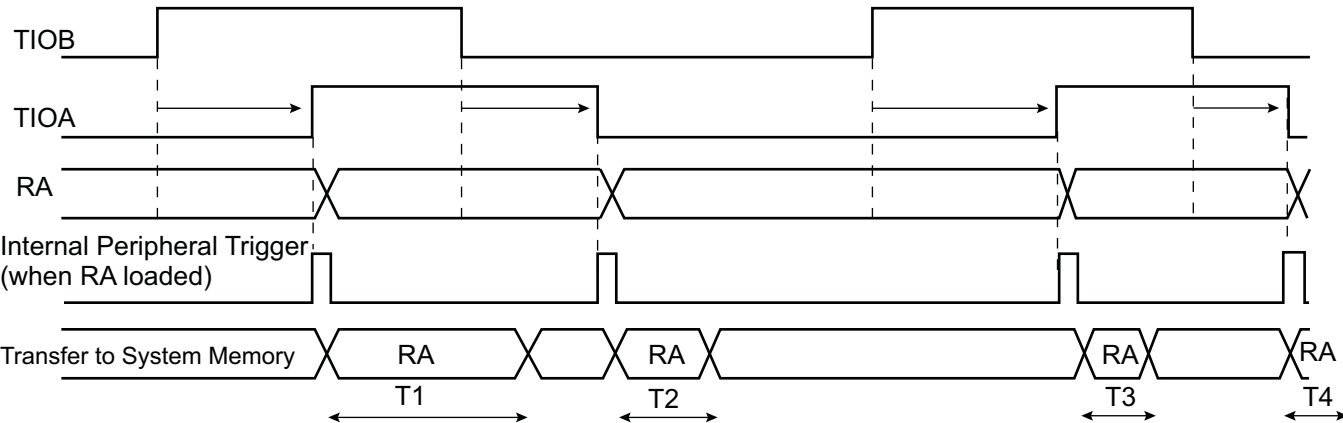


ETRGEDG = 1, LDRA = 1, LDRB = 2, ABETRG = 0



T1, T2, T3, T4 = System Bus load dependent ( $t_{\min} = 8$  Peripheral Clocks)

ETRGEDG = 3, LDRA = 3, LDRB = 0, ABETRG = 0



T1, T2, T3, T4 = System Bus load dependent ( $t_{\min} = 8$  Peripheral Clocks)