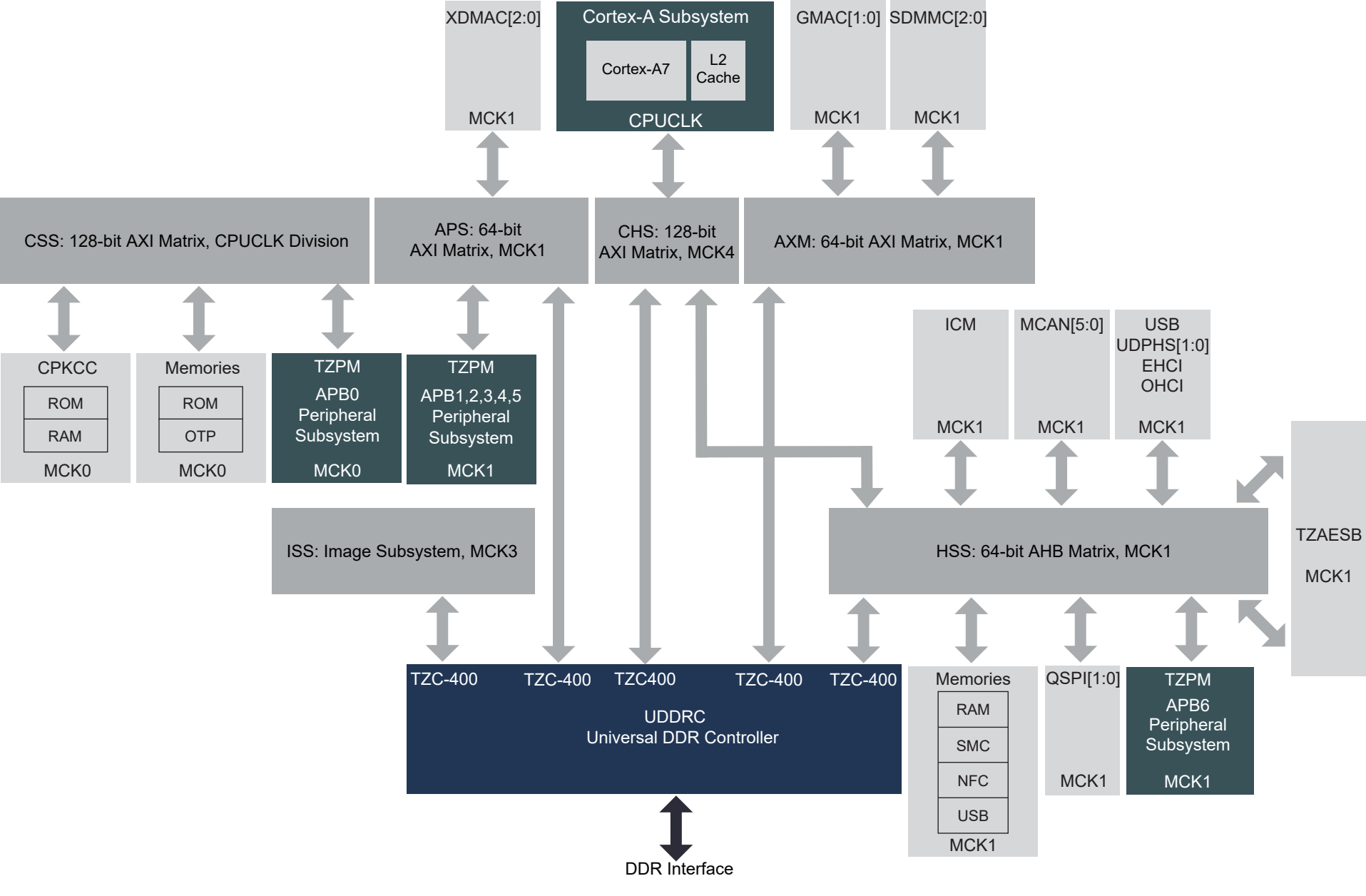
XDMAC[2:0]
MCK1
Cortex-A Subsystem
Cortex-A7
L2 Cache
CPUCLK
GMAC[1:0]
MCK1
SDMMC[2:0]
MCK1
CSS: 128-bit AXI Matrix, CPUCLK Division
APS: 64-bit AXI Matrix, MCK1
CHS: 128-bit AXI Matrix, MCK4
AXM: 64-bit AXI Matrix, MCK1
CPKCC
ROM
RAM
MCK0
Memories
ROM
OTP
MCK0
TZPM
APB0 Peripheral Subsystem
MCK0
TZPM
APB1,2,3,4,5 Peripheral Subsystem
MCK1
ICM
MCK1
MCAN[5:0]
MCK1
USB
UDPHS[1:0]
EHCI
OHCI
MCK1
ISS: Image Subsystem, MCK3
HSS: 64-bit AHB Matrix, MCK1
TZAESB
MCK1
TZC-400
TZC-400
TZC400
TZC-400
TZC-400
UDDRC
Universal DDR Controller
Memories
RAM
SMC
NFC
USB
MCK1
QSPI[1:0]
MCK1
TZPM
APB6 Peripheral Subsystem
MCK1
DDR Interface