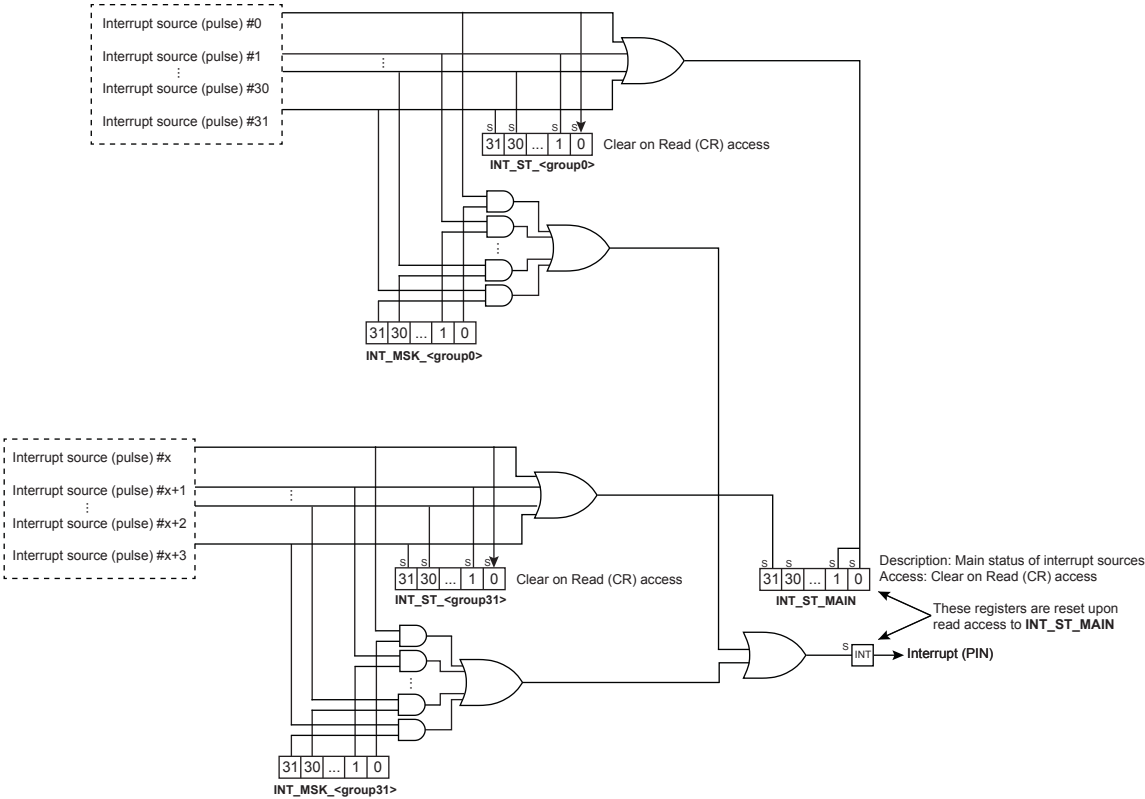
Interrupt source (pulse) #0
Interrupt source (pulse) #1
Interrupt source (pulse) #30
Interrupt source (pulse) #31
31 30 ... 1 0
Clear on Read (CR) access
INT_ST_<group0>
31 30 ... 1 0
INT_MSK_<group0>
Interrupt source (pulse) #x
Interrupt source (pulse) #x+1
Interrupt source (pulse) #x+2
Interrupt source (pulse) #x+3
31 30 ... 1 0
Clear on Read (CR) access
INT_ST_<group31>
31 30 ... 1 0
INT_MSK_<group31>
31 30 ... 1 0
INT_ST_MAIN
Description: Main status of interrupt sources
Access: Clear on Read (CR) access
These registers are reset upon read access to INT_ST_MAIN
INT
Interrupt (PIN)