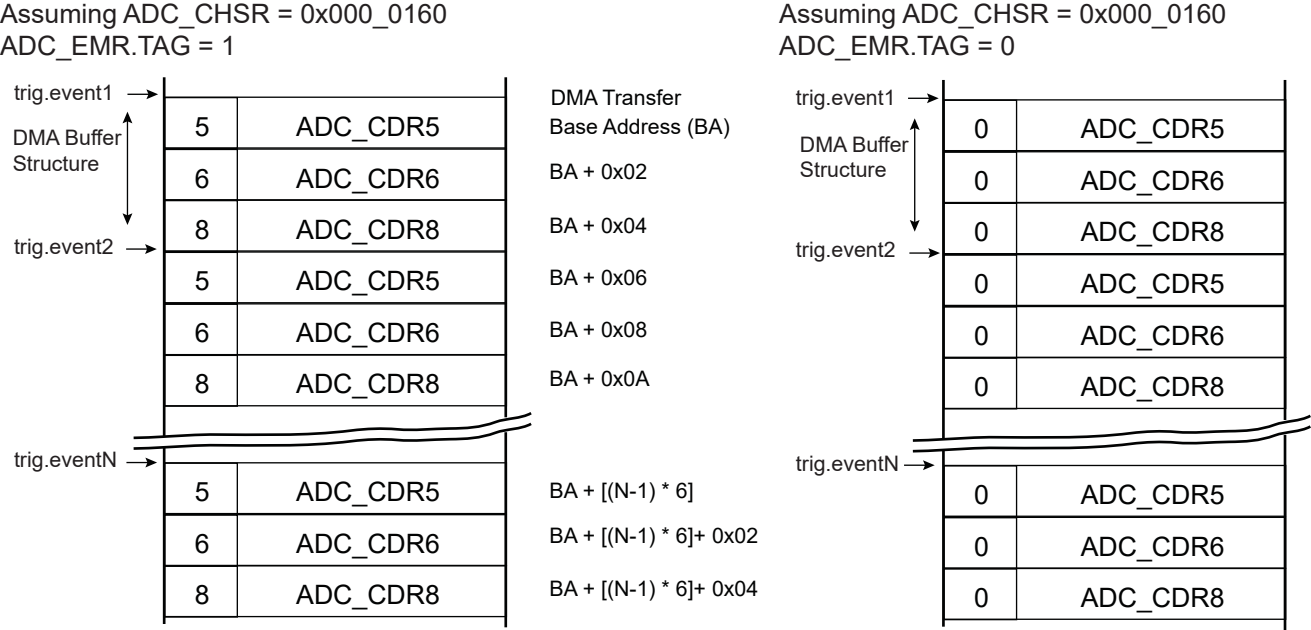
Assuming ADC_CHSR = 0x000_0160
ADC_EMR.TAG = 1
trig.event1
DMA Buffer Structure
trig.event2
trig.eventN
5 ADC_CDR5
6 ADC_CDR6
8 ADC_CDR8
5 ADC_CDR5
6 ADC_CDR6
8 ADC_CDR8
5 ADC_CDR5
6 ADC_CDR6
8 ADC_CDR8
DMA Transfer Base Address (BA)
BA + 0x02
BA + 0x04
BA + 0x06
BA + 0x08
BA + 0x0A
BA + [(N-1) * 6]
BA + [(N-1) * 6]+ 0x02
BA + [(N-1) * 6]+ 0x04
Assuming ADC_CHSR = 0x000_0160
ADC_EMR.TAG = 0
trig.event1
DMA Buffer Structure
trig.event2
trig.eventN
0 ADC_CDR5
0 ADC_CDR6
0 ADC_CDR8
0 ADC_CDR5
0 ADC_CDR6
0 ADC_CDR8
0 ADC_CDR5
0 ADC_CDR6
0 ADC_CDR8