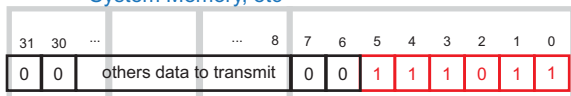


6 valid bits on data (SPDIFTX_MR.VBPS = 6)
1-byte CDR container (SPDIFTX_MR.BPS = 0)

Note: Little-Endian mode

System Memory, etc



valid data = LSB justified

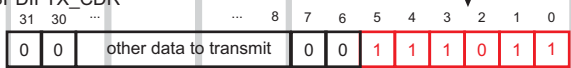


SPDIFTX

SPDIFTX_MR.JUSTIFY=0

BPS=0

SPDIFTX_CDR

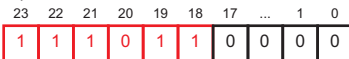


shift

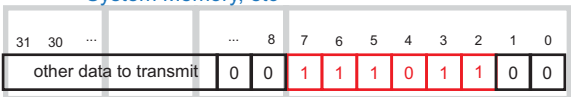


SPDIF frame

First transmitted data



System Memory, etc



valid data = MSB justified



SPDIFTX

SPDIFTX_MR.JUSTIFY=1

BPS=0

SPDIFTX_CDR



shift



SPDIF frame

First transmitted data

