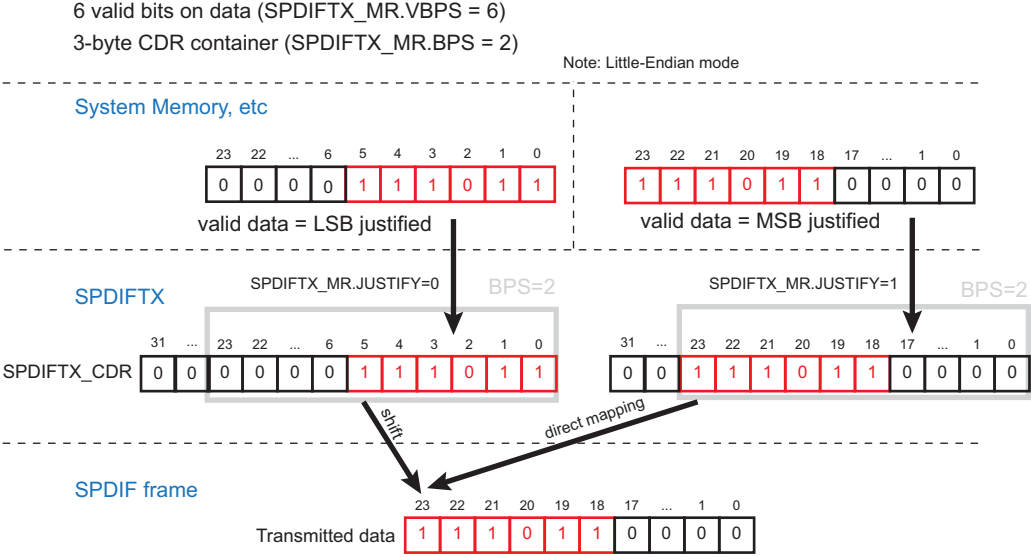
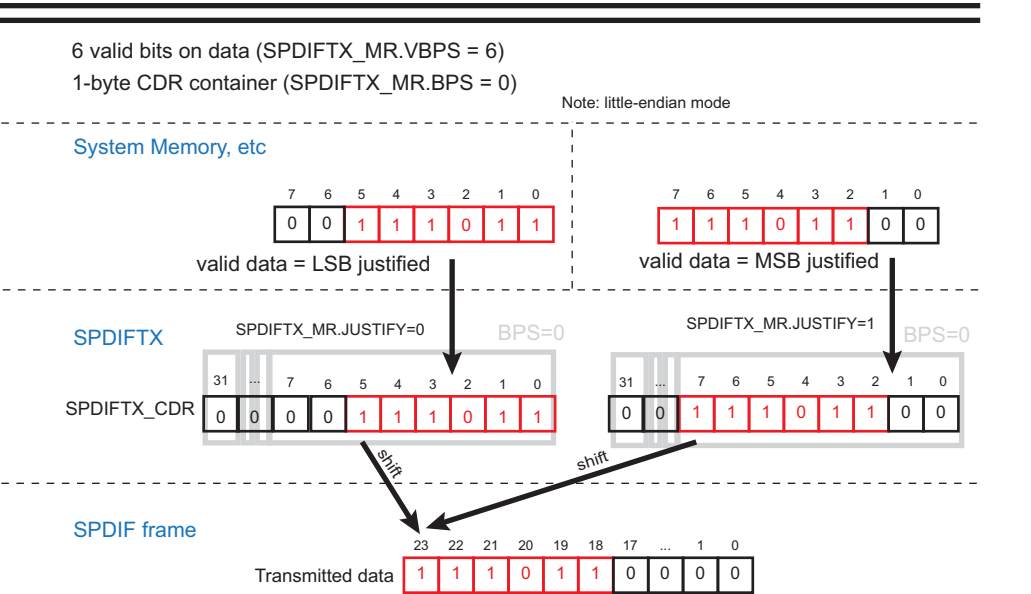

6 valid bits on data (SPDIFTX_MR.VBPS = 6)
3-byte CDR container (SPDIFTX_MR.BPS = 2)
Note: Little-Endian mode
System Memory, etc
23 22 ... 6 5 4 3 2 1 0
0 0 0 0 1 1 1 0 1 1
valid data = LSB justified
23 22 21 20 19 18 17 ... 1 0
1 1 1 0 1 1 0 0 0 0
valid data = MSB justified
SPDIFTX
SPDIFTX_MR.JUSTIFY=0
BPS=2
SPDIFTX_MR.JUSTIFY=1
BPS=2
SPDIFTX_CDR
31 ... 23 22 ... 6 5 4 3 2 1 0
0 0 0 0 0 0 1 1 1 0 1 1
31 ... 23 22 21 20 19 18 17 ... 1 0
0 0 1 1 1 0 1 1 0 0 0 0
shift
direct mapping
SPDIF frame
Transmitted data
23 22 21 20 19 18 17 ... 1 0
1 1 1 0 1 1 0 0 0 0


6 valid bits on data (SPDIFTX_MR.VBPS = 6)
1-byte CDR container (SPDIFTX_MR.BPS = 0)
Note: little-endian mode
System Memory, etc
7 6 5 4 3 2 1 0
0 0 1 1 1 0 1 1
valid data = LSB justified
7 6 5 4 3 2 1 0
1 1 1 0 1 1 0 0
valid data = MSB justified
SPDIFTX
SPDIFTX_MR.JUSTIFY=0
BPS=0
SPDIFTX_MR.JUSTIFY=1
BPS=0
SPDIFTX_CDR
31 ... 7 6 5 4 3 2 1 0
0 0 0 0 1 1 1 0 1 1
31 ... 7 6 5 4 3 2 1 0
0 0 1 1 1 0 1 1 0 0
shift
shift
SPDIF frame
Transmitted data
23 22 21 20 19 18 17 ... 1 0
1 1 1 0 1 1 0 0 0 0