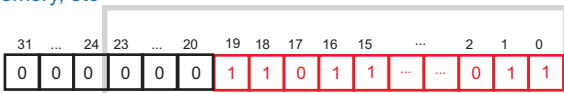


20 valid bits on data (SPDIFTX_MR.VBPS = 20)
3-byte CDR container (SPDIFTX_MR.BPS = 2)

Note: Little-Endian mode

System Memory, etc



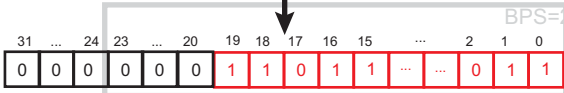
valid data = LSB justified

SPDIFTX

SPDIFTX_CDR

SPDIFTX_MR.JUSTIFY=0

BPS=2

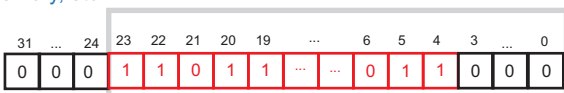


SPDIF frame

First transmitted data



System Memory, etc



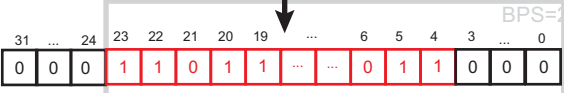
valid data = MSB justified

SPDIFTX

SPDIFTX_CDR

SPDIFTX_MR.JUSTIFY=1

BPS=2



SPDIF frame

First transmitted data

