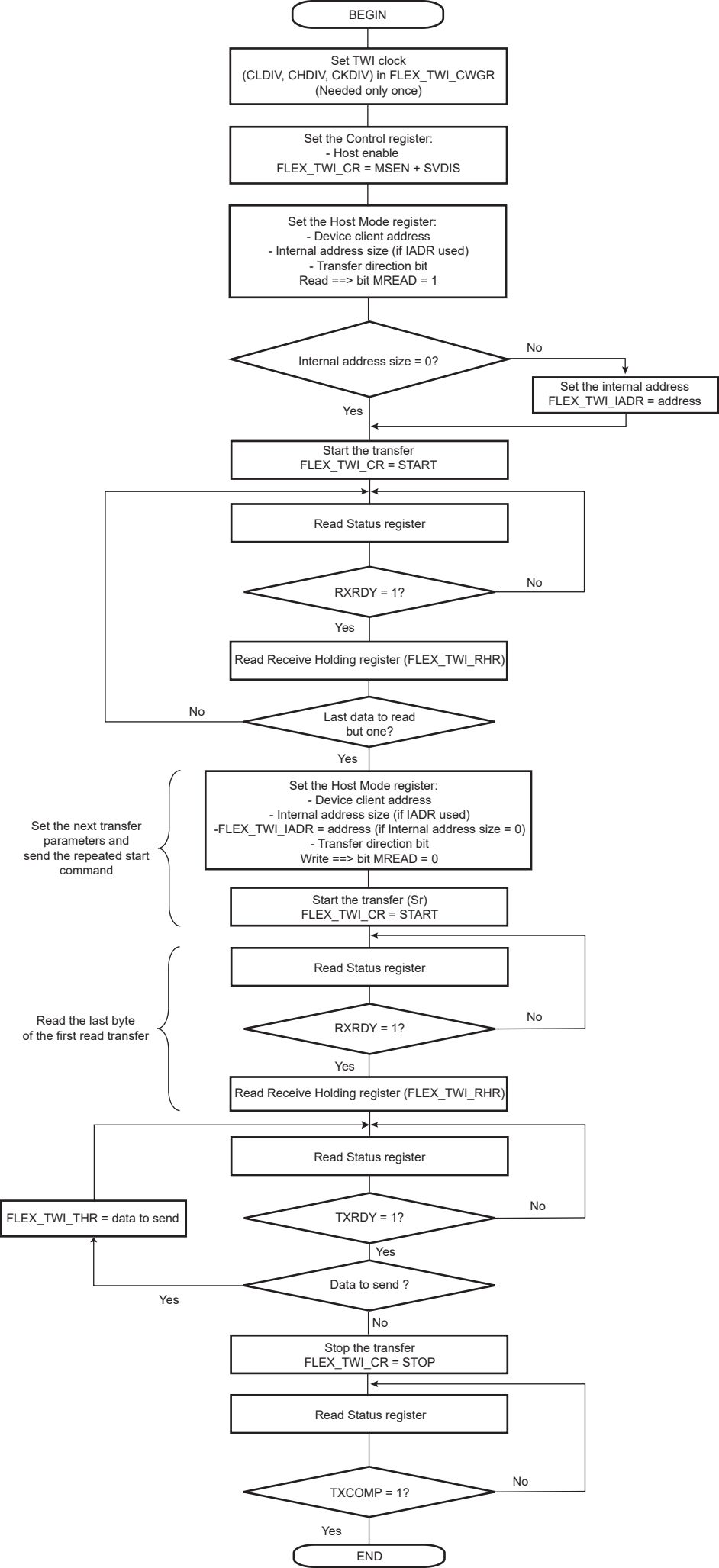
BEGIN
Set TWI clock
(CLDIV, CHDIV, CKDIV) in FLEX_TWI_CWGR
(Needed only once)
Set the Control register:
- Host enable
FLEX_TWI_CR = MSEN + SVDIS
Set the Host Mode register:
- Device client address
- Internal address size (if IADR used)
- Transfer direction bit
Read ==> bit MREAD = 1
Internal address size = 0?
No
Set the internal address
FLEX_TWI_IADR = address
Yes
Start the transfer
FLEX_TWI_CR = START
Read Status register
RXRDY = 1?
No
Yes
Read Receive Holding register (FLEX_TWI_RHR)
Last data to read
but one?
No
Yes
Set the next transfer
parameters and
send the repeated start
command
Set the Host Mode register:
- Device client address
- Internal address size (if IADR used)
-FLEX_TWI_IADR = address (if Internal address size = 0)
- Transfer direction bit
Write ==> bit MREAD = 0
Start the transfer (Sr)
FLEX_TWI_CR = START
Read the last byte
of the first read transfer
Read Status register
RXRDY = 1?
No
Yes
Read Receive Holding register (FLEX_TWI_RHR)
Read Status register
FLEX_TWI_THR = data to send
TXRDY = 1?
No
Yes
Data to send ?
Yes
No
Stop the transfer
FLEX_TWI_CR = STOP
Read Status register
TXCOMP = 1?
No
Yes
END