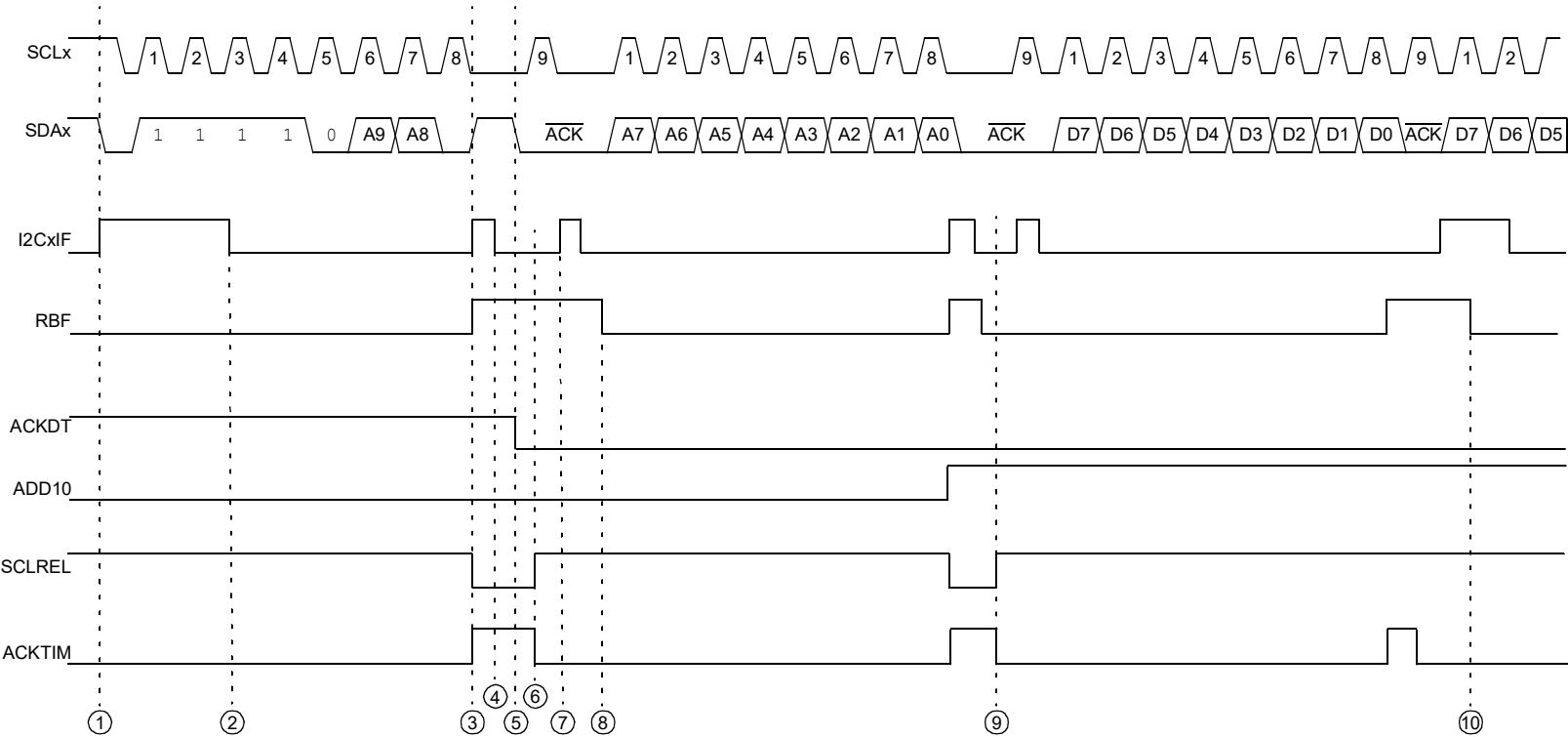

① Detecting the Start bit enables address detection; interrupt is set if the SCEN bit is set.

② User software clears the interrupt flag.

③ Client receives first address byte. Write indicated. Interrupt flag is asserted. ACKTIM is asserted. If AHEN = 1, client suspends clock. SCLREL is cleared by hardware.

④ User software clears the interrupt flag.

⑤ ACKDT is written with $\overline{\text{ACK}}$ by user software.

⑥ User software sets SCLREL to release clock hold.

⑦ Client interrupt is asserted.

⑧ User software reads I2CxRCV buffer, that clears RBF flag.

⑨ Client Acknowledges the second address byte.

⑩ User software reads data from the I2CxRCV register.