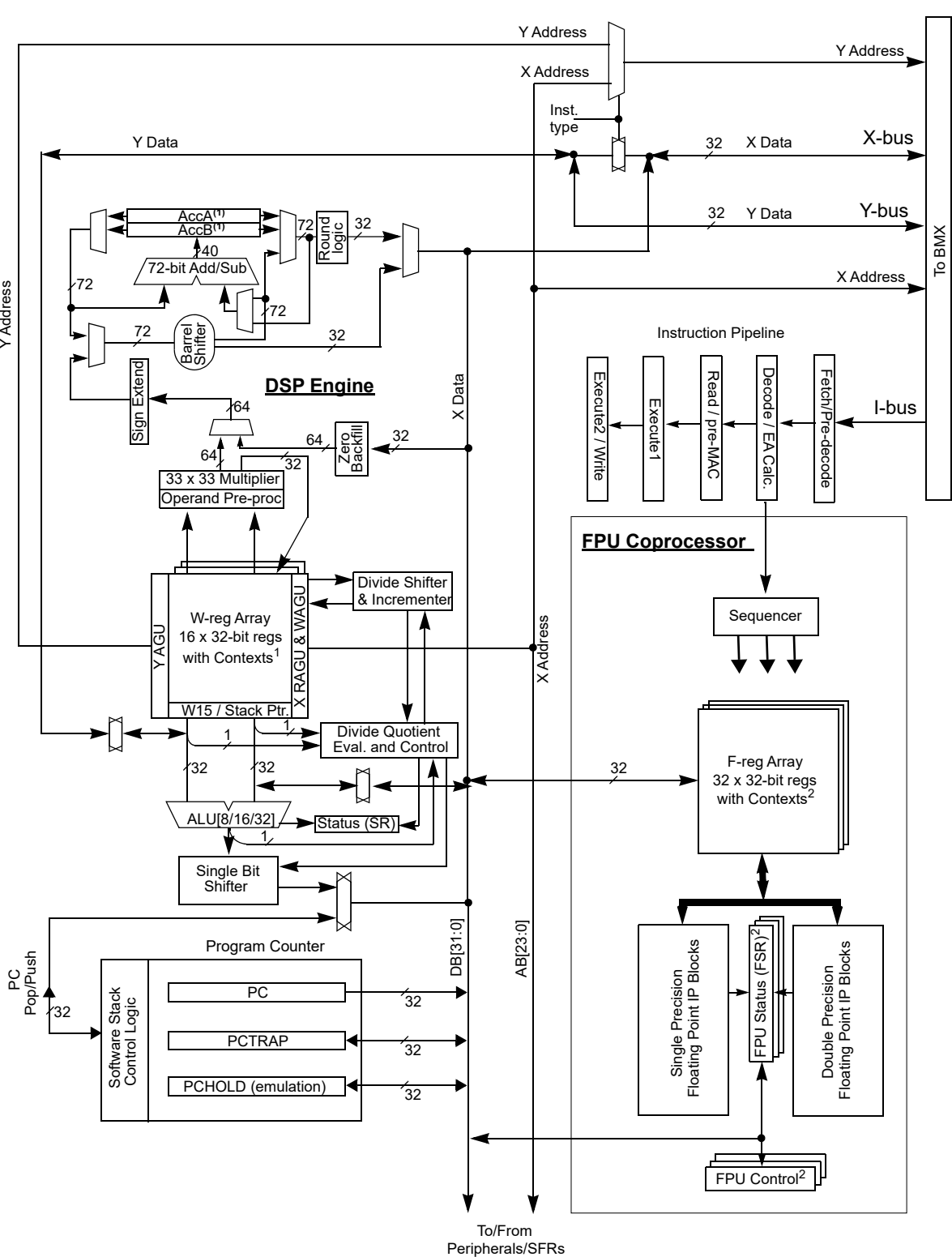
Y Address
X Address
Inst. type
Y Address
Y Data
32
X Data
X-bus
32
Y Data
Y-bus
To BMX
X Address
AccA(1)
AccB(1)
72
Round logic
32
40
72-bit Add/Sub
72
72
72
Barrel Shifter
32
Y Address
Sign Extend
64
DSP Engine
X Data
64
64
32
Zero Backfill
32
33 x 33 Multiplier
Operand Pre-proc
Instruction Pipeline
Execute2 / Write
Execute1
Read / pre-MAC
Decode / EA Calc.
Fetch/Pre-decode
I-bus
FPU Coprocessor
Divide Shifter & Incrementer
Y AGU
W-reg Array
16 x 32-bit regs
with Contexts1
X RAGU & WAGU
W15 / Stack Ptr.
X Address
Sequencer
1
1
1
Divide Quotient Eval. and Control
32
32
32
F-reg Array
32 x 32-bit regs
with Contexts2
ALU[8/16/32]
Status (SR)
1
Single Bit Shifter
Program Counter
PC Pop/Push
32
Software Stack Control Logic
PC
PCTRAP
PCHOLD (emulation)
32
32
32
DB[31:0]
AB[23:0]
Single Precision Floating Point IP Blocks
FPU Status (FSR)2
Double Precision Floating Point IP Blocks
FPU Control2
To/From Peripherals/SFRs