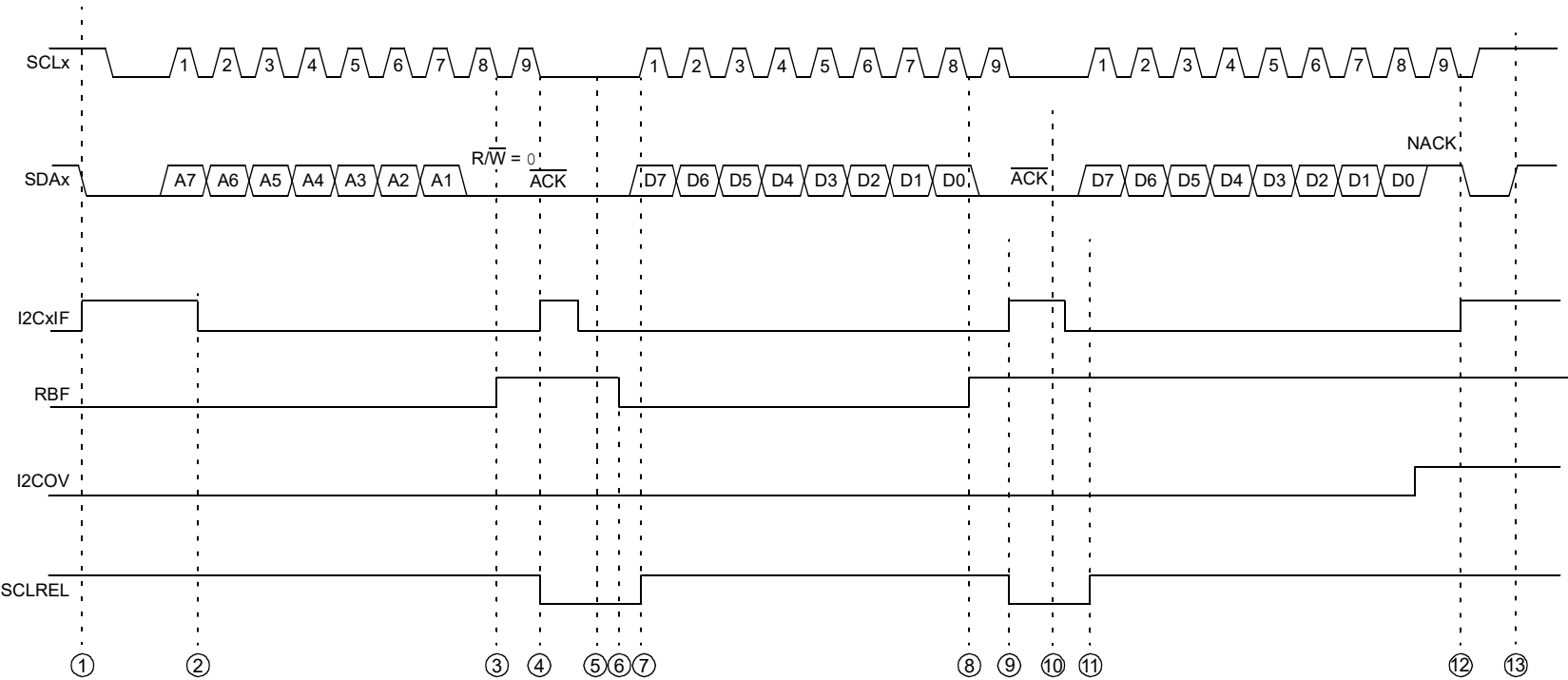

① Detecting Start bit, enables address detection, interrupt is set if SCEN is set.

② User software clears the interrupt flag.

③ RBF is set on the 8th falling clock, address is loaded into I2CxRCV. RBF is asserted.

④ Interrupt is asserted.

⑤ SCLx is stretched low until SCLREL is set.

⑥ User software reads the I2CxRCV buffer, that clears the RBF flag.

⑦ User software releases the SCLx line by writing SCLREL to '1'.

⑧ Data is loaded into I2CxRCV. RBR flag is asserted.

⑨ On the 9th falling clock edge, interrupt is asserted.

⑩ SCLx is stretched and held low until SCLREL is set.

⑪ User software releases SCLx line by writing SCLREL to '1'.

⑫ NACK is received (SCLx is not stretched to low).

⑬ Client recognizes the Stop event.