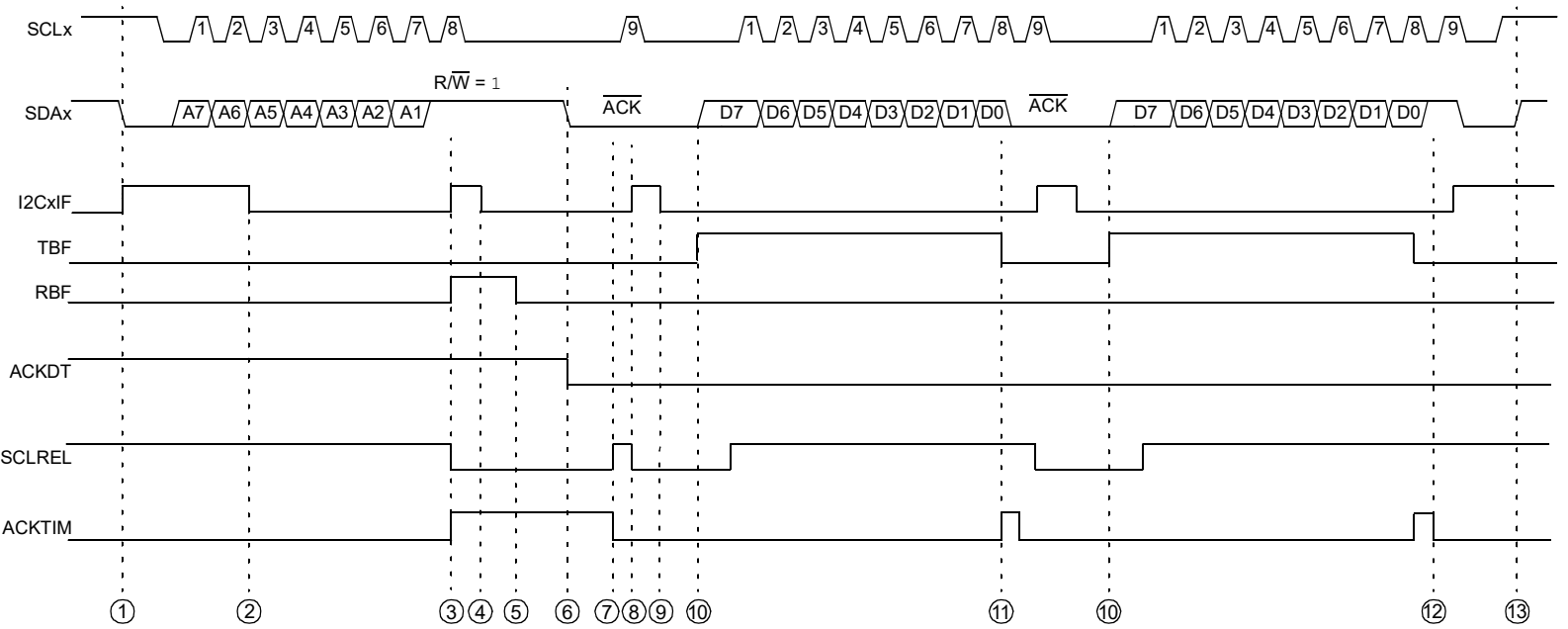

① Detecting Start bit enables address detection, interrupt is set if the SCIE bit is set.

② User software clears the interrupt flag.

③ Client receives the address byte with R/$\overline{W}$ = 1. Hardware clears SCLREL to suspend host clock. ACKTIM and interrupt flag are asserted.

④ User software clears the interrupt flag.

⑤ Software reads the I2CxRV register, that clears the RBF flag.

⑥ ACKDT is written with $\overline{ACK}$.

⑦ User software sets SCLREL to release clock hold. Host clocks in the Acknowledgment sequence. ACKTIM is cleared by hardware.

⑧ Hardware clears SCLREL to suspend host clock if R/$\overline{W}$ = 1.

⑨ User software clears the interrupt flag.

⑩ User software loads the I2CxTRN register with response data. TBF = 1 indicates that the buffer is full.

⑪ After last bit, module clears TBF bit, indicating buffer is available for next byte.

⑫ At the end of ninth clock, if host sent NACK, no more data is expected. Module does not suspend the clock.

⑬ Module recognizes Stop event.