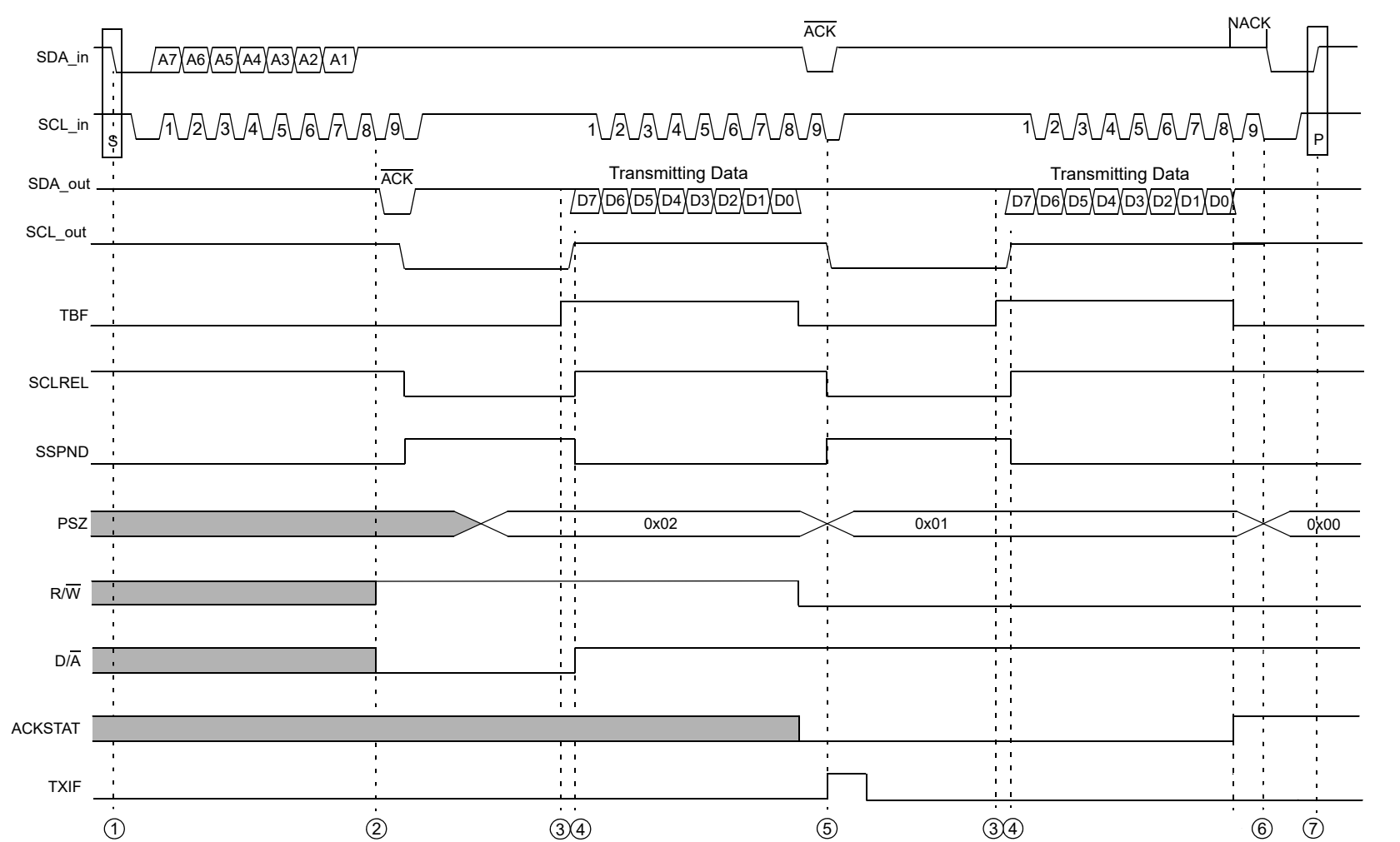

① Client recognizes Start event, S and P bits set/clear accordingly.

② Client receives address byte. Address matches. Address byte is moved to I2CxRCV register and is read by user software to prevent buffer overflow. R/W = 1 to indicate read from Client.

③ User software writes I2CxTRN with response data. TBF = 1 indicates that buffer is full. Writing I2CxTRN sets D/$\overline{A}$, indicating a data byte.

④ SCLREL will be set by hardware automatically to release the clock. SCLREL will be released after data setup if configured. SSPND will be cleared to indicate clock release.

⑤ I2CxTXIF will be set after transmitting data.

⑥ EOP will be set.

⑦ Client recognizes Stop event; S and P bits set/clear accordingly.