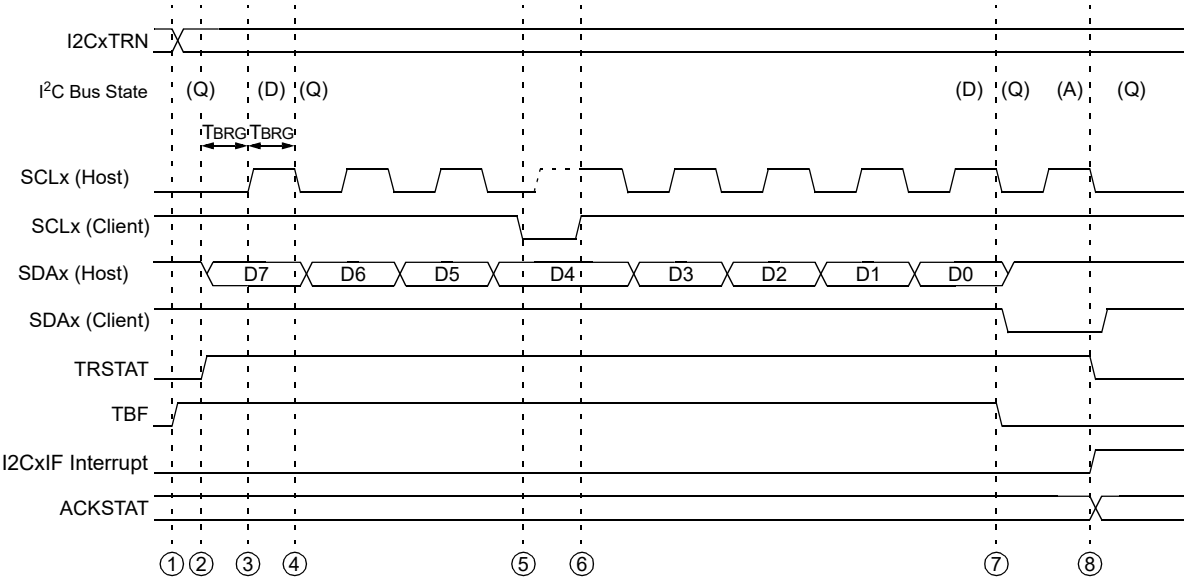

① Writing to the I2CxTRN register will start a host transmission event. The TBF status bit is set.

② The BRG starts. The MSB of the I2CxTRN register drives SDAx. SCLx remains low. The TRSTAT status bit is set.

③ The BRG times out. SCLx is released and the BRG restarts.

④ The BRG times out. SCLx is driven low. After SCLx is detected low, the next bit of the I2CxTRN register drives SDAx.

⑤ While SCLx is low, the client can also pull SCLx low to initiate a Wait (clock stretch).

⑥ Host has already released SCLx and client can release to end the Wait . The BRG restarts.

⑦ At the falling edge of the eighth SCLx clock, the host releases SDAx. The TBF status bit is cleared.
The client drives an $\overline{\text{ACK}}$/NACK

⑧ At the falling edge of the ninth SCLx clock, the host generates the interrupt. SCLx remains low until the next event.
The client releases SDAx and the TRSTAT status bit is clear.