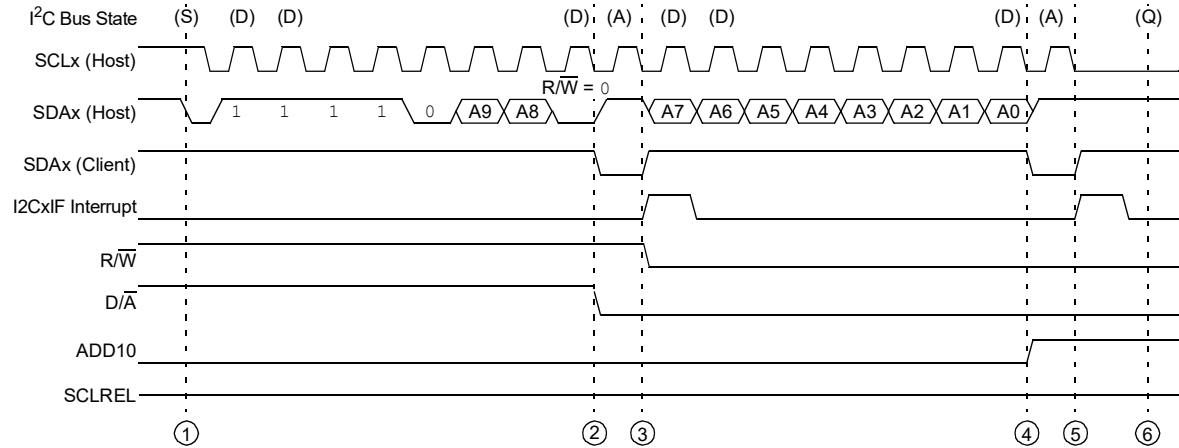

(1) Detecting the Start bit enables address detection.

(2) Address match of first byte clears the D/$\overline{A}$ status bit and causes client logic to generate an $\overline{ACK}$.

(3) Reception of first byte clears the R/$\overline{W}$ status bit. Client logic generates an interrupt.

(4) Address match of first and second byte sets the ADD10 status bit and causes client logic to generate an $\overline{ACK}$.

(5) Reception of second byte completes the 10-bit address. Client logic generates an interrupt.