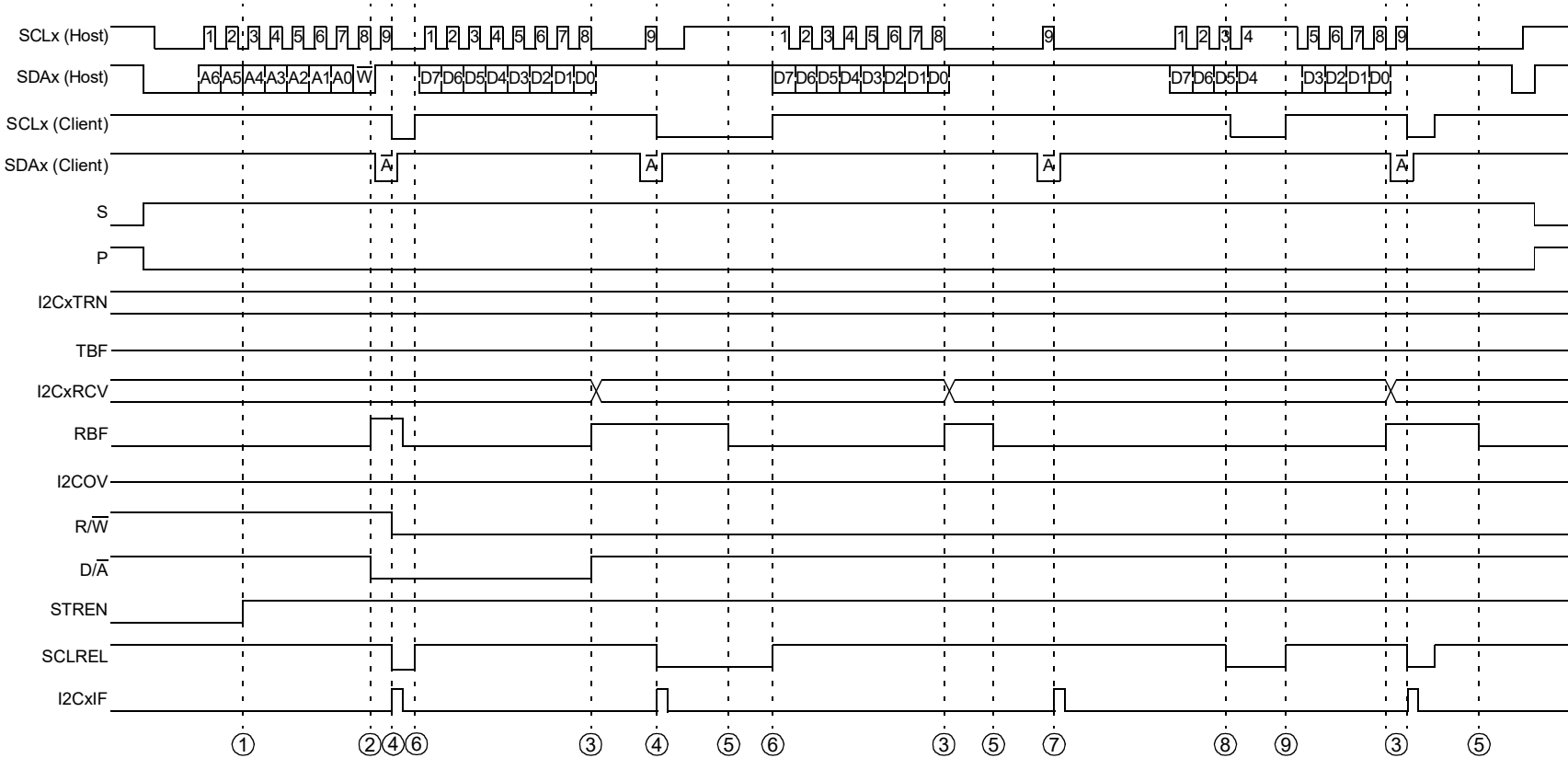

① User software sets the STREN bit to enable clock stretching.

② Client receives address byte. I2CxRCV register is read by user software to prevent buffer overflow.

③ Next received byte is message data. The byte moves to the I2CxRCV register, sets RBF.

④ Because RBF = 1 at ninth clock, automatic clock stretch begins. Client clears SCLREL bit. Client pulls SCLx line low to stretch clock.

⑤ User software reads I2CxRCV register. RBF bit clears.

⑥ User software sets SCLREL bit to release clock.

⑦ Client does not clear SCLREL because RBF = 0 at this time.

⑧ User software may clear SCLREL to cause a clock hold. Module must detect SCLx low before asserting SCLx low.

⑨ User software may set SCLREL to release a clock hold.