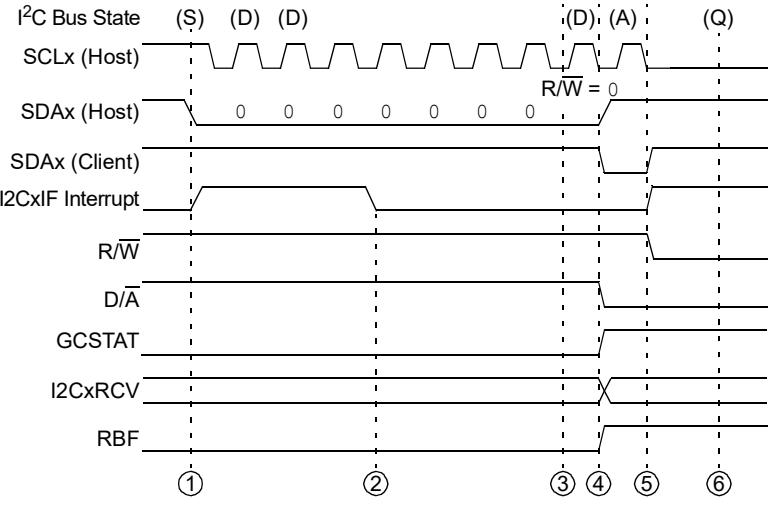

1. Detecting Start bit enables address detection. If SCIE is set, then interrupt will be asserted.(1)
2. User software clears the interrupt flag.(1)
3. All '0's and R/$\overline{W}$ = 0 indicates a general call.
4. Valid address clears D/$\overline{A}$ status bit and sets GCSTAT status bit. Client generates $\overline{ACK}$. Address is loaded into I2CxRCV register.
5. R/$\overline{W}$ status bit cleared. Client generates an interrupt.
6. Bus waiting. Client is ready to receive data.