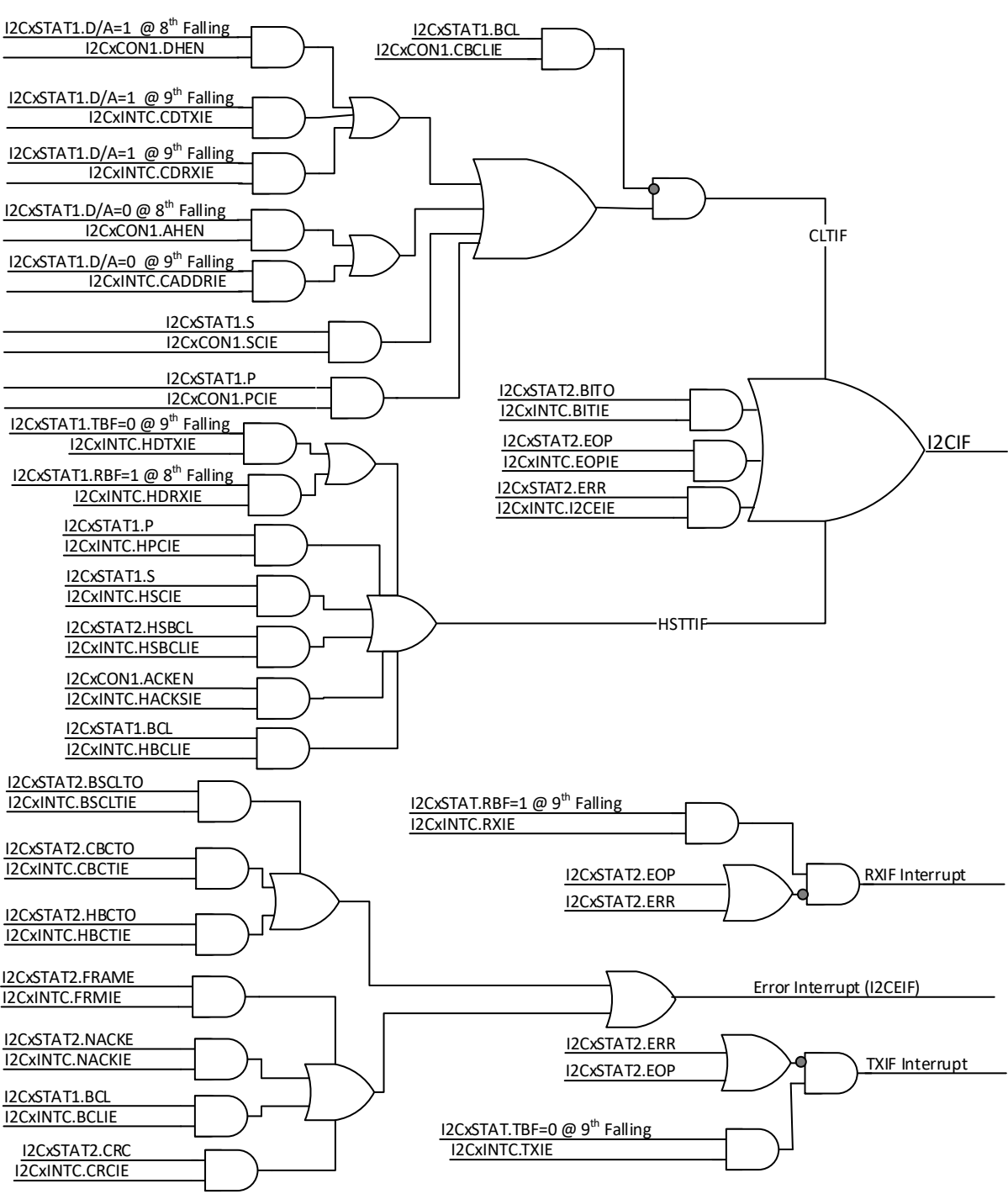

- The Receive interrupt will be generated when EOP=1 to read the last byte by DMA
- The First Transmit Data byte write is expected write by the CPU
- The Transmit interrupt is not generated after the last byte Transmit
- The HACKSIE control the ACK Sequence completion interrupt generated at @9th falling edge after transmitting the ACK|NACK in the host receive mode.
- The TXIF,RXIF and I2CEIF are not in the status bits, those are actual interrupt outputs.
- Data transmission interrupt is not generated to get CRC value from CPU or DMA in the CRC Auto append mode since the transmitted CRC value is already present in the CRC calculator.