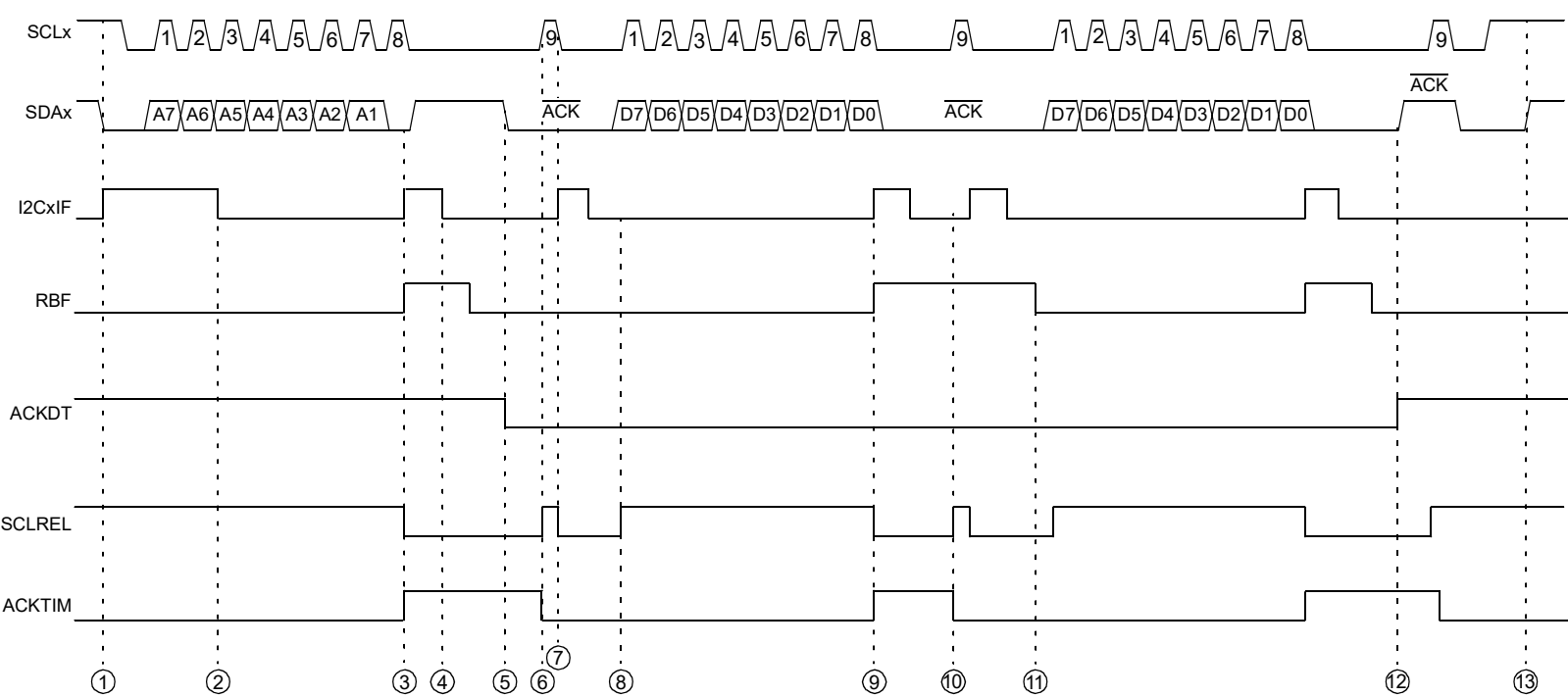

① Detecting Start bit, enables address detection, interrupt is set if SCEN is set.

② User software clears the interrupt flag.

③ Client receives first address byte. Write Indicated. If AHEN = 1, SCLREL is cleared by hardware. ACKTIM and interrupt are asserted.

④ User software clears the interrupt flag.

⑤ ACKDT is written with an $\overline{\text{ACK}}$ by user software.

⑥ User software sets SCLREL to release the clock hold; ACKTIM is cleared by hardware.

⑦ Hardware stretches the clock after $\overline{\text{ACK}}$ (if STREN = 1).

⑧ User software sets SCLREL to release clock hold.

⑨ I2CxRCV is loaded with I2CxRSR. RBF is set. If DHEN = 1, SCLREL is cleared by hardware and ACKTIM is asserted.

⑩ User software sets SCLREL to release the clock hold. ACKTIM is cleared by hardware. After Acknowledgment, hardware stretches the clock.

⑪ User software reads I2CxRCV, that clears the RBF flag.

⑫ NACK sent by host.

⑬ Module recognizes the Stop event.