Bit	15	14	13	12	11	10	9	8
	CNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 - CNT[15:0] Byte Count

Condition	Description
If receiving data:	Count value decremented on 8th falling SCL edge when a new byte is loaded into I2CxRXB
If transmitting data:	Count value decremented on 9th falling SCL edge when a new byte is moved into I2CxTXB

Notes:

1. It is recommended to write this register only when the module is Idle (MMA = 0 or SMA = 0) or when the module is clock stretching (CSTR = 1 or MDR = 1).

2. CNTIF is set on the 9th falling SCL edge when I2CxCNT = 0.

3. I2CxCNTH is double-buffered for writing and must be written to before writing to I2CxCNTL. The counter value is updated when I2CxCNTL is written.