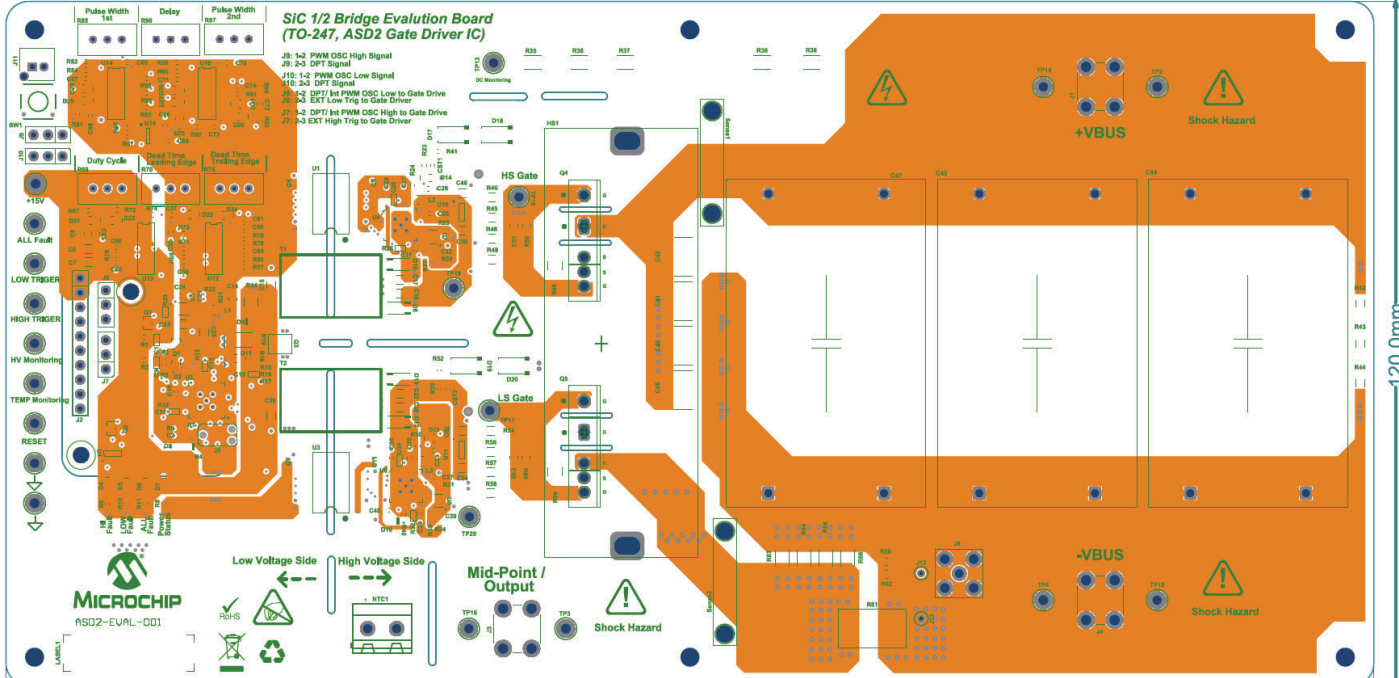


SiC 1/2 Bridge Evaluation Board (TO-247, ASD2 Gate Driver IC)



Pulse Width Test (R33, R34, R35)

Delay (R36, R37, R38)

Pulse Width 2nd (R39, R40, R41)

Duty Cycle (R42, R43, R44)

Dead Time Leading Edge (R45, R46, R47)

Dead Time Trailing Edge (R48, R49, R50)

+15V

ALL Fault

LOW TRIGGER

HIGH TRIGGER

HV Monitoring

TEMP Monitoring

RESET

MICROCHIP
ASD2-EVAL-001

Low Voltage Side ←

High Voltage Side →

Mid-Point / Output

RoHS, RECYCLE, NTC1

- J9: 1-2 PWM OSC High Signal
- J9: 2-3 DPT Signal
- J10: 1-2 PWM OSC Low Signal
- J10: 2-3 DPT Signal
- J6: 1-2 DPT/Int PWM OSC Low to Gate Drive
- J6: 2-3 EXT Low Trig to Gate Drive
- J7: 1-2 DPT/Int PWM OSC High to Gate Drive
- J7: 2-3 EXT High Trig to Gate Drive

DC Monitoring

R33, R34, R35, R36, R37, R38, R39

HS Gate

Q4, D4, R42, R43, R44, R45, R46, R47, R48, R49, R50

LS Gate

Q5, D5, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60

+V_{BUS}

TP13, TP14, TP15

Shock Hazard

DC Link

C43, C44, C45

-V_{BUS}

TP16, TP17, TP18

Shock Hazard

240.0mm

120.0mm