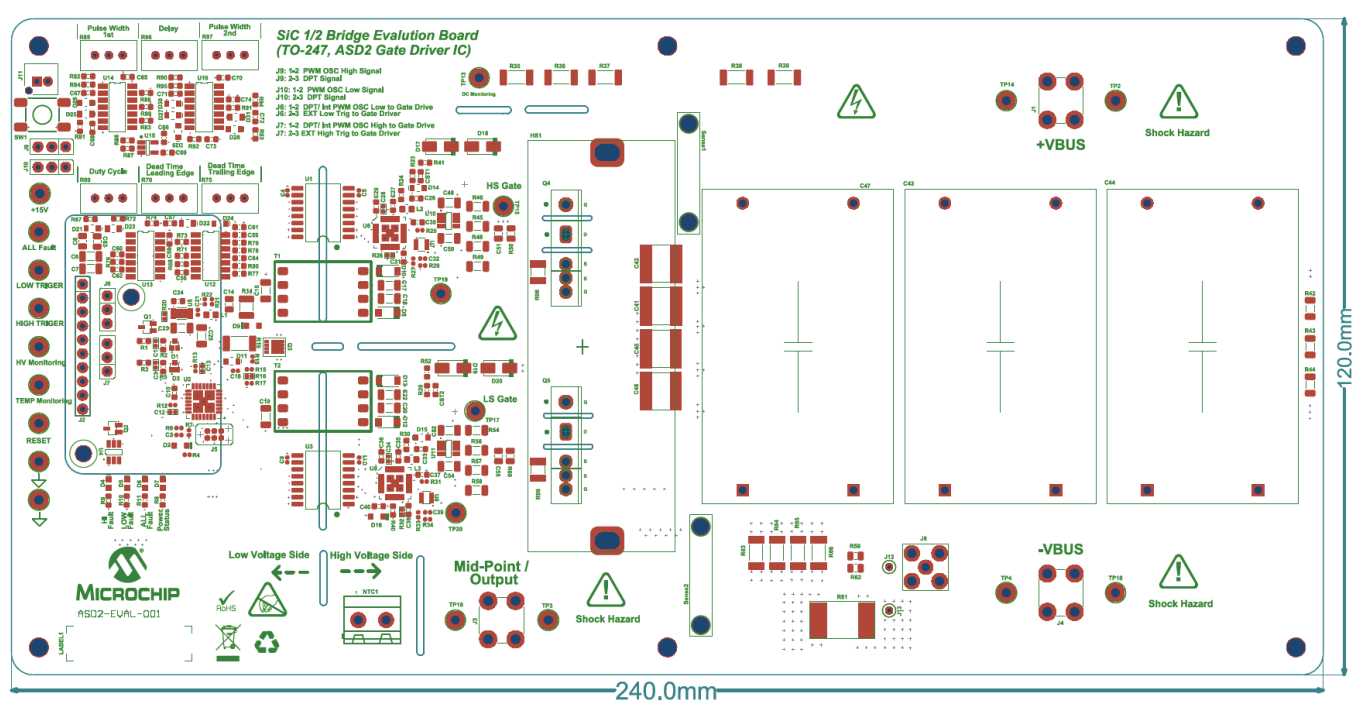
SiC 1/2 Bridge Evalution Board
(TO-247, ASD2 Gate Driver IC)
J9: 1-2 PWM OSC High Signal
J9: 2-3 DPT Signal
J10: 1-2 PWM OSC Low Signal
J10: 2-3 DPT Signal
J6: 1-2 DPT/ Int PWM OSC Low to Gate Drive
J6: 2-3 EXT Low Trig to Gate Driver
J7: 1-2 DPT/ Int PWM OSC High to Gate Drive
J7: 2-3 EXT High Trig to Gate Driver
Pulse Width 1st
Delay
Pulse Width 2nd
Duty Cycle
Dead Time Leading Edge
Dead Time Trailing Edge
+15V
ALL Fault
LOW TRIGER
HIGH TRIGER
HV Monitoring
TEMP Monitoring
RESET
HS Gate
LS Gate
Mid-Point / Output
+VBUS
-VBUS
Shock Hazard
Low Voltage Side
High Voltage Side
MICROCHIP
ASD2-EVAL-001
240.0mm
120.0mm