BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63	
1C00h		1C80h		1D00h		1D80h		1E00h		1E80h		1F00h		1F80h	
	Core Registers		Core Registers		Core Registers		Cara Bagistars		Core Registers		Core Registers		Core Registers		Cara Bagistars
	Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers
1C0Bh		1C8Bh		1D0Bh		1D8Bh		1E0Bh		1E8Bh		1F0Bh		1F8Bh	
1C0Ch		1C8Ch		1D0Ch		1D8Ch		1E0Ch	UMTOAP	1E8Ch		1F0Ch		1F8Ch	
								1E0Dh	UMTOAL						
								1E0Eh	UMTOAH						
								1E0Fh							
															Unimplemented
															Read as '0'
											See Table 2 for		See Table 3 for		
	Unimplemented		Unimplemented		Unimplemented		Unimplemented				register mapping		register mapping		
	Read as '0'		Read as '0'		Read as '0'		Read as '0'		Unimplemented		details		details		
									Read as '0'					1FE3h	
														1FE4h	STATUS SHAD
														1FE5h	WREG_SHAD
														1FE6h	BSR_SHAD
														1FE7h	PCLATH_SHAD
														1FE8h	FSR0L_SHAD
														1FE9h 1FEAh	FSR0H_SHAD
														1FEBh	FSR1L_SHAD FSR1H SHAD
														1FECh	- TSKITI_STAD
														1FEDh	STKPTR
														1FEEh	TOSL
1C6Fh		1CEFh		1D6Fh		1DEFh		1E6Fh		1EEFh		1F6Fh		1FEFh	TOSH
1C70h	Common RAM	1CF0h	Common RAM	1D70h	Common RAM	1DF0h	Common RAM	1E70h	Common RAM	1EF0h	Common RAM	1F70h	Common RAM	1FF0h	Common RAM
	(Accesses		(Accesses		(Accesses		(Accesses		(Accesses		(Accesses		(Accesses		(Accesses
1C7Fh	70h-7Fh)	1CFFh	70h-7Fh)	1D7Fh	70h-7Fh)	1DFFh	70h-7Fh)	1E7Fh	70h-7Fh)	1EFFh	70h-7Fh)	1F7Fh	70h-7Fh)	1FFFh	70h-7Fh)
1.	Legend:														
1 '	-	ented da	ta memory locations	s, read as	'0'										