BANK 62

1F00h	Core Registers	1F30h	RE0PPS[1]	1F57h	—
		1F31h	RE1PPS[1]	1F58h	—
1F0Bh		1F32h	RE2PPS[1]	1F59h	ANSELD[1]
1F0Ch	Unimplemented Read as '0'	1F33h	RE3PPS	1F5Ah	WPUD[1]
		1F34h	Unimplemented Read as '0'	1F5Bh	ODCOND[1]
1F0Fh				1F5Ch	SLRCOND[1]
1F10h	RA0PPS	1F37h		1F5Dh	INLVLD[1]
1F11h	RA1PPS	1F38h	ANSELA	1F5Eh	Unimplemented Read as '0'
1F12h	RA2PPS	1F39h	WPUA		
1F13h	RA3PPS	1F3Ah	ODCONA	1F63h	
1F14h	RA4PPS	1F3Bh	SLRCONA	1F64h	ANSELE
1F15h	RA5PPS	1F3Ch	INLVLA	1F65h	WPUE
1F16h	RA6PPS	1F3Dh	IOCAP	1F66h	ODCONE
1F17h	RA7PPS	1F3Eh	IOCAN	1F67h	SLRCONE
1F18h	RB0PPS	1F3Fh	IOCAF	1F68h	INLVLE
1F19h	RB1PPS	1F40h	Unimplemented Read as '0'	1F69h	IOCEP
1F1Ah	RB2PPS			1F6Ah	IOCEN
1F1Bh	RB3PPS	1F42h		1F6Bh	IOCEF
1F1Ch	RB4PPS	1F43h	ANSELB	1F6Ch	Unimplemented Read as '0'
1F1Dh	RB5PPS	1F44h	WPUB		
1F1Eh	RB6PPS	1F45h	ODCONB	1F6Fh	
1F1Fh	RB7PPS	1F46h	SLRCONB	1F70h	Common RAM (Accesses 70h-7Fh)
1F20h	RC0PPS	1F47h	INLVLB		
1F21h	RC1PPS	1F48h	IOCBP	1F7Fh	
1F22h	RC2PPS	1F49h	IOCBN		
1F23h	RC3PPS	1F4Ah	IOCBF		
1F24h	RC4PPS	1F4Bh	Unimplemented Read as '0'		
1F25h	RC5PPS				
1F26h	RC6PPS	1F4Dh			
1F27h	RC7PPS	1F4Eh	ANSELC		
1F28h	RD0PPS[1]	1F4Fh	WPUC		
1F29h	RD1PPS[1]	1F50h	ODCONC		
1F2Ah	RD2PPS[1]	1F51h	SLRCONC		
1F2Bh	RD3PPS[1]	1F52h	INLVLC		
1F2Ch	RD4PPS[1]	1F53h	IOCCP		
1F2Dh	RD5PPS[1]	1F54h	IOCCN		
1F2Eh	RD6PPS[1]	1F55h	IOCCF		
1F2Fh	RD7PPS[1]	1F56h	—		

Note: 1. Available on 40-pin devices only.

Legend:

Unimplemented data memory locations, read as '0'