

MPLAB X IDE v6.20 - getting_started_sam_d21_xpro: sam_d21_xpro

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Resource Management [MCC] x

MCC v5.5.1

Project Resource... Gener... Impor... Exp... ?

Libraries

- Harmony
 - Packs
 - Peripherals
- System
 - System

Device Resources

Content Manager

Libraries

- Harmony
 - Board Support Packages (BSPs)
 - Bootloader
 - Core
 - Drivers
 - Graphics
 - Input
 - Libraries
 - Peripherals
 - System Services
 - TCP/IP
 - Third Party Libraries
 - Tools
 - Touch
 - USB

Start Page x Project Graph x **Clock Easy View** x

Oscillators Controller

8 MHz Internal Oscillator

$\div 1$

FREQ/1

OSC8M

XIN

8,000,000

XOUT

Crystal Oscillator

CRYSTAL

XOSC

Fractional Digital Phase Locked Loop (FDPLL)

Clock Source GCLK0

GCLK_DRL

$\times 2$

XOSC32K

$\times 1.0$

0

0

Auto Calculate

FDPLL

Digital Frequency Locked Loop (DRLL 48MHz)

Clock Source GCLK0

GCLK_DRL

Calib

Open

DCO

$\times 1$

1

48,000,000 Hz

DRLL

32 KHz Oscillators Controller

32K High Accuracy Internal Oscillator

OSC32K

OSCULP32K

GCLK Generator 0

XOSC

OSC8M

FDPLL

DRL

OSCULP32K

OSC32K

XOSC3K

GCLK_IN[0]

GCLK1

$\div 1$

1

DPLL

GCLK0

48,000,000 Hz

Main Clock

$\div 1$

DIV1

48,000,000 Hz

CPU

GCLK Generator 1

XOSC

OSC8M

FDPLL

DRL

OSCULP32K

OSC32K

XOSC3K

GCLK_IN[1]

OSCULP32K

$\div 32$

32

GCLK1

1,024 Hz

Peripheral Clock Selection

GCLK0

GCLK1

GCLK2

GCLK3

GCLK4

GCLK5

GCLK6

GCLK7

GCLK8

Peripheral Clock Configuration

Peripherals

GCLK Generator x (x=2-8)

XOSC

OSC8M

FDPLL

DRL

OSCULP32K

OSC32K

XOSC3K

GCLK_IN[0]

GCLK1

$\div 1$

1

DPLL

GCLK2

GCLK3

GCLK4

GCLK5

GCLK6

GCLK7

GCLK8

GCLKx

GCLK I/O Configuration

GCLK_IN[x]

GCLKx

GCLK_I/O[x]

Output x Notifications [MCC] x News

EDBG x Scripting x MPLAB® Code Configurator x