Timer Setup:
    START = Either ERS Edge   RESET = At Start+PR Match   STOP = At PR Match
    CSYNC = Sync

Note:
1. Cross-domain clock synchronization applies as required but is not highlighted.
2. A synchronous edge-triggered Start/Stop condition is one timer clock cycle wide internally. Multiple consecutive edges in short interval of time may cause the internal Start/Stop condition to remain set for a longer time duration.
3. The RUN trace illustrates the internal Timer Clock domain run/stop signal. Clock sync delays apply before the value appears in the RUN SFR bit.
4. The uncertainty of the output is due to the prescaler setting.
5. Cleared by software.