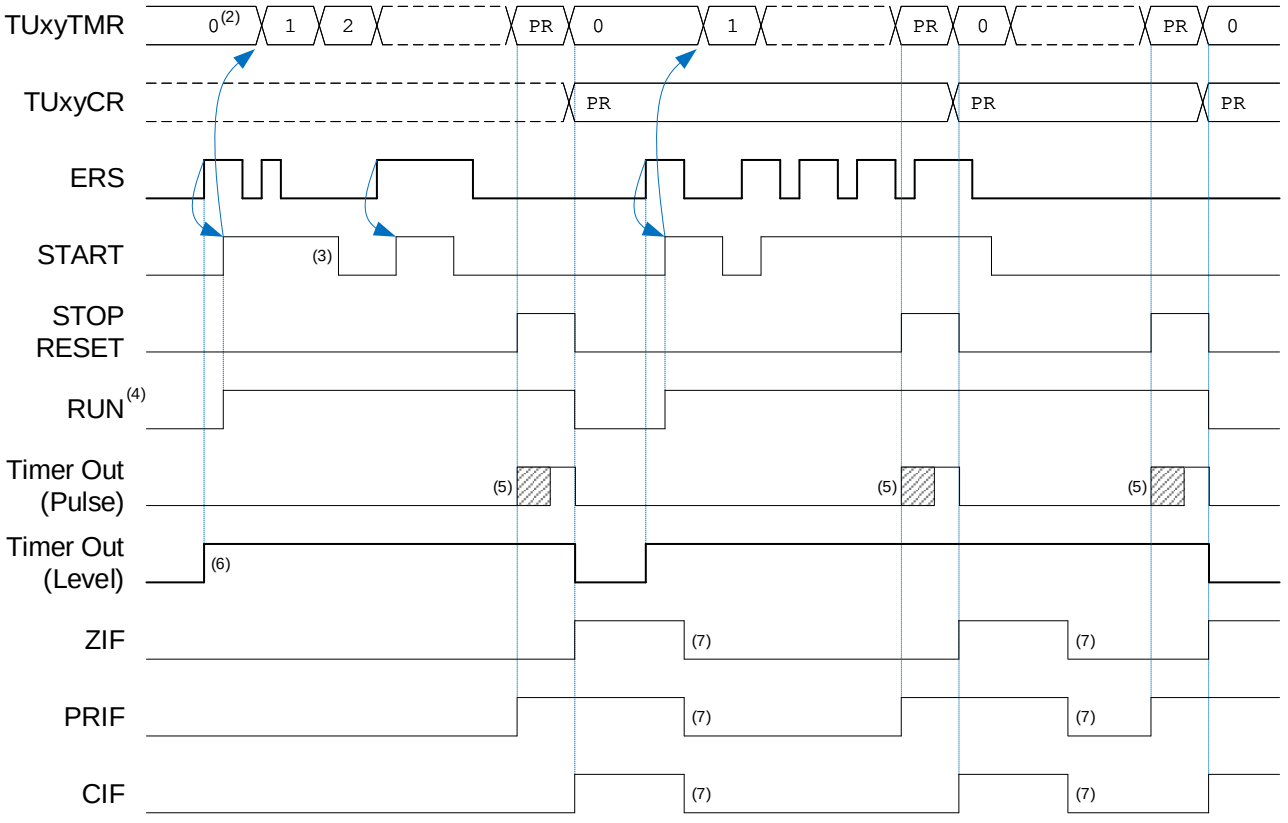

Timer Setup:

START = Rising ERS Edge RESET = At PR Match STOP = At PR Match
CSYNC = Sync

Note:

1. Cross-domain clock synchronization applies as required but is not highlighted.
2. Ensure that TUxyTMR counter is reset to zero by setting CLR command.
3. A synchronous edge-triggered Start/Stop condition is one timer clock cycle wide internally. Multiple consecutive edges in short interval of time may cause the internal Start/Stop condition to remain set for a longer time duration.
4. The RUN trace illustrates the internal Timer Clock domain run/stop signal. Clock sync delays apply before the value appears in the RUN SFR bit.
5. The uncertainty of the output is due to the prescaler setting.
6. Timer Out (Level) rises along with ERS when START = Rising/Either ERS Edge.
7. Cleared by software.