



### Timer Setup:

START = None (ON = 1)  
CSYNC = Sync

RESET = ERS Level-0+PR Match  
OSEN = Enabled

STOP = Either ERS Edge

### Note:

1. Cross-domain clock synchronization applies as required but is not highlighted.
2. The ON bit is set in the software and cleared by hardware upon Stop (one-shot mode).
3. The RUN trace illustrates the internal Timer Clock domain run/stop signal. Clock sync delays apply before the value appears in the RUN SFR bit.
4. The uncertainty of the output is due to the prescaler setting.
5. Cleared by software.