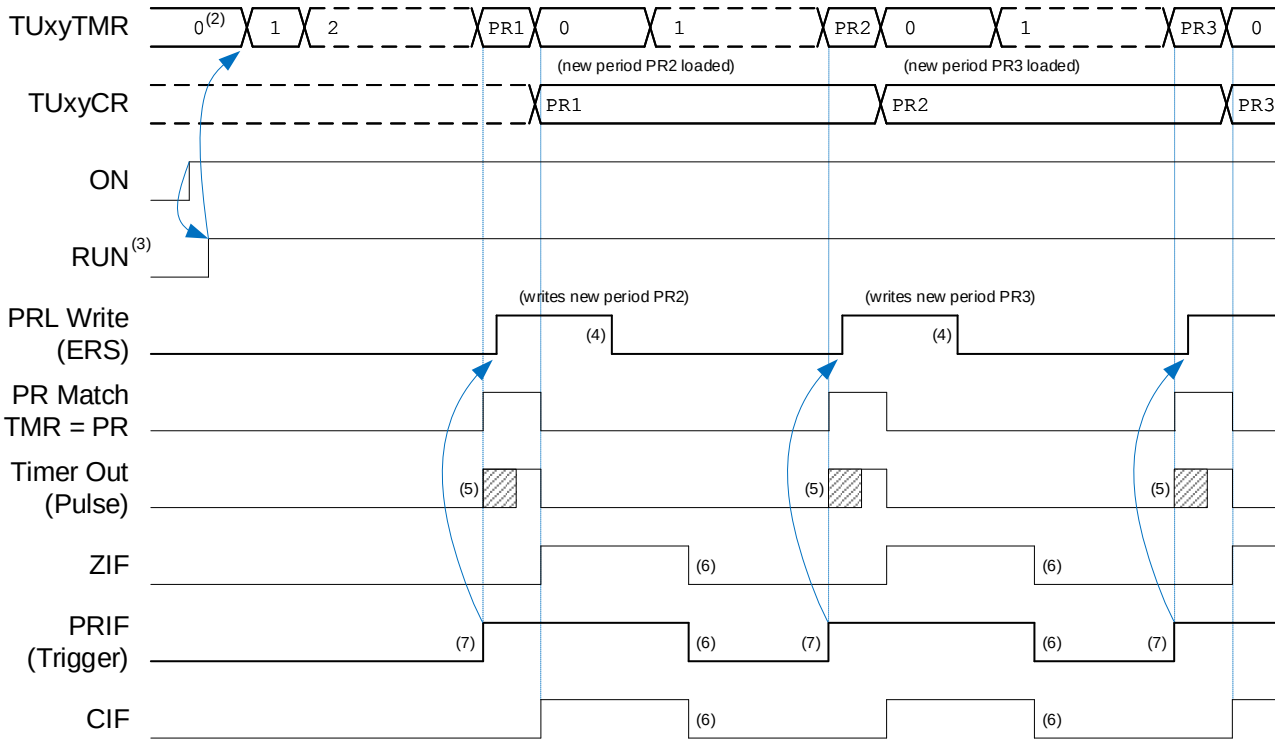

Timer Setup:

START = None (ON = 1)	RESET = ERS Level-0+PR Match	STOP = None
CSYNC = Sync	ERS = PRL_Write	EPOL = Inverted

Note:

1. Cross-domain clock synchronization applies as required but is not highlighted.
2. Ensure that TUxyTMR counter is reset to zero by setting CLR command.
3. The RUN trace illustrates the internal Timer Clock domain run/stop signal. Clock sync delays apply before the value appears in the RUN SFR bit.
4. The PRL_Write signal stays asserted for up to two timer clock cycles internally.
5. The uncertainty of the output is due to the prescaler setting.
6. Cleared by software.
7. PRIF is used as a DMA trigger to write to TUxyPR register.