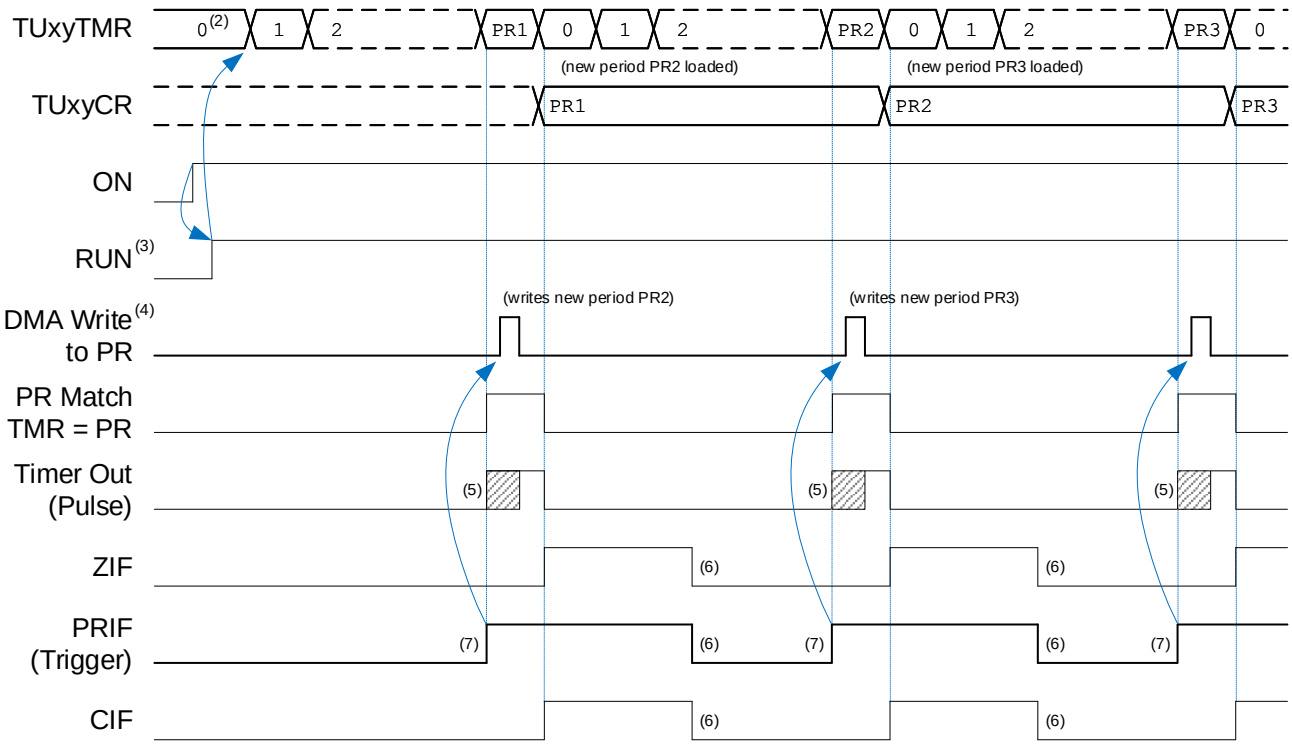

Timer Setup:

START = None (ON = 1) RESET = At PR Match STOP = None
CSYNC = Sync

Note:

1. Cross-domain clock synchronization applies as required but is not highlighted.
2. Ensure that TUxyTMR counter is reset to zero by setting CLR command.
3. The RUN trace illustrates the internal Timer Clock domain run/stop signal. Clock sync delays apply before the value appears in the RUN SFR bit.
4. DMA write signal is based on instruction clock. In the figure, the instruction clock (Fosc/4) is assumed to be faster than the timer clock. If the timer clock is faster than the instruction clock, then the DMA write will take longer than the PR match duration and the period may not update until the next PR match event.
5. The uncertainty of the output is due to the prescaler setting.
6. Cleared by software.
7. PRIF is used as a DMA trigger to write to TUxyPR register.