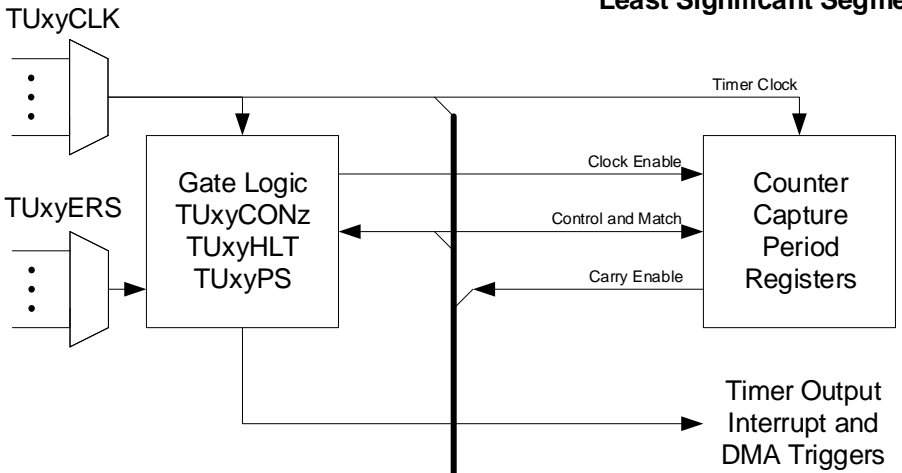


Least Significant Segment



Timer Chain Out

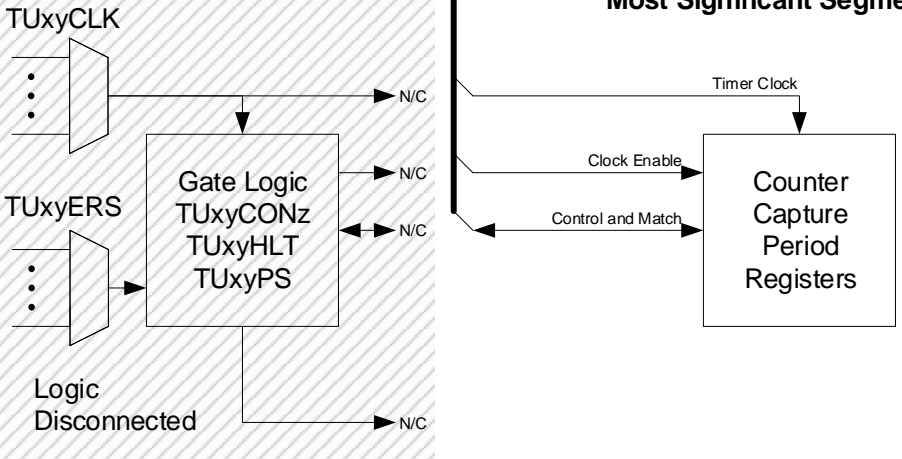
TUCHAIN

Master

Slave

Timer Chain In

Most Significant Segment



Note:

1. This is a conceptual diagram only.
2. Control registers, state machine, prescaler and input ERS and clock for slave is not used. Rather they are derived from the master segment.