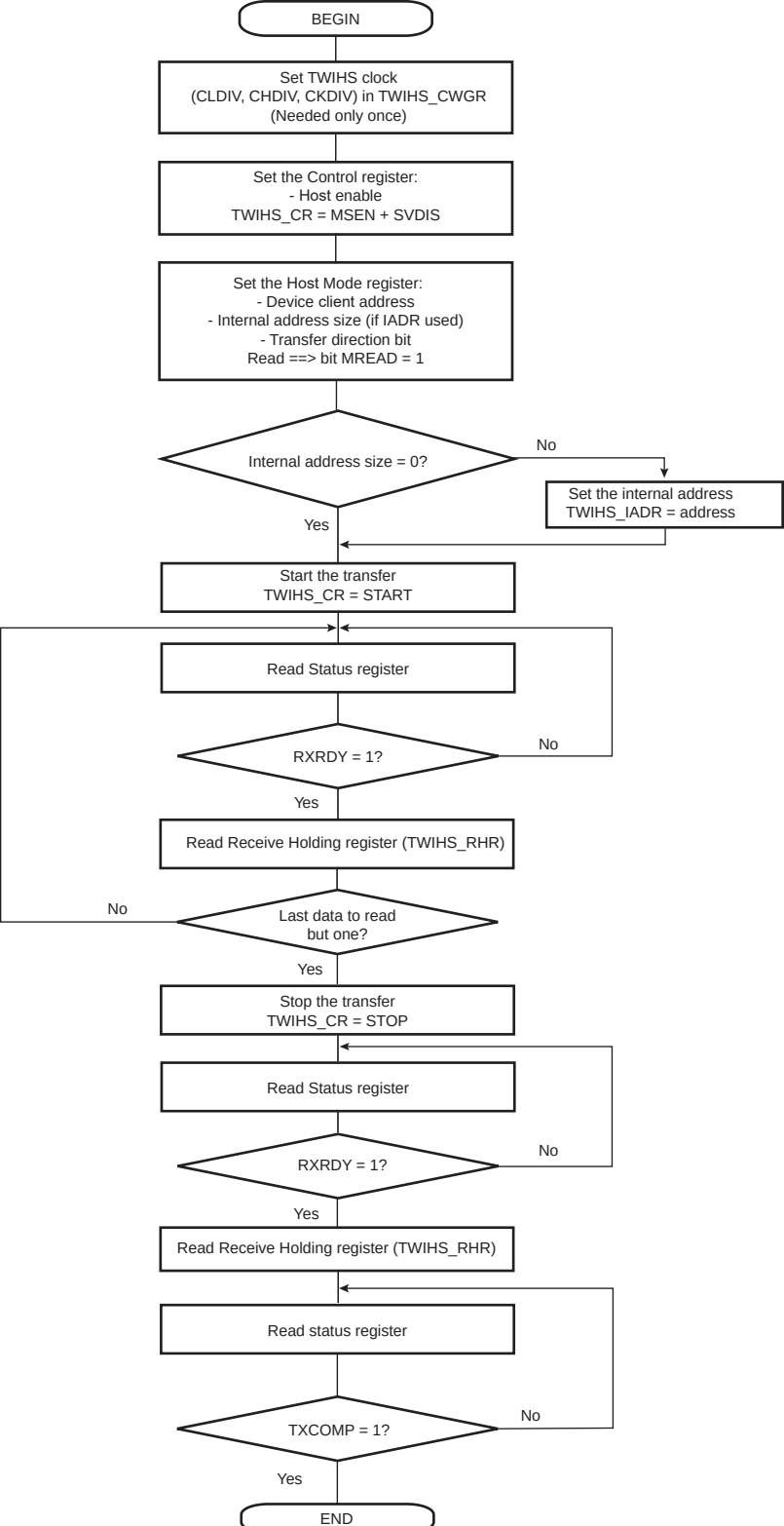
BEGIN
Set TWIHS clock
(CLDIV, CHDIV, CKDIV) in TWIHS_CWGR
(Needed only once)
Set the Control register:
- Host enable
TWIHS_CR = MSEN + SVDIS
Set the Host Mode register:
- Device client address
- Internal address size (if IADR used)
- Transfer direction bit
Read ==> bit MREAD = 1
Internal address size = 0?
No
Set the internal address
TWIHS_IADR = address
Yes
Start the transfer
TWIHS_CR = START
Read Status register
RXRDY = 1?
No
Yes
Read Receive Holding register (TWIHS_RHR)
No
Last data to read
but one?
Yes
Stop the transfer
TWIHS_CR = STOP
Read Status register
RXRDY = 1?
No
Yes
Read Receive Holding register (TWIHS_RHR)
Read status register
TXCOMP = 1?
No
Yes
END