Channel x slected clock CHIDx(PWM_SR) CHIDx(PWM_ENA) CHIDx(PWM_DIS) Left Alianed CALG(PWM_CMRx) = 0 PWM_CCNTx CPRD(PWM_CPRDx) CDTY(PWM CDTYx) Output Waveforms Period PWM CMRx Software configurations CPOL = 0 CPOL = 1 DPOLI = 0 DPOLI = 0 DTE = 0 DTE = 0 PPM = 1 PPM = 1 DTOHx DTHI = 0 DTHI = 1 DTLI = 0 DTLI = 1 DTOLx T I. I DTOHx DTHI = 0DTHI = 1 DTLI = 1 DTLI = 0 DTOLX 1 DTOHx DTHI = 1 DTHI = 0 DTLI = 0 DTLI = 1 DTOLx I. L Ĩ ī DTOHx DTHI = 1DTHI = 0DTLI = 1 DTLI = 0 DTOLx I PWM_CMRx Software configurations CPOL = 0 CPOL = 1 DPOLI = 1 DPOLI = 1 DTE = 0DTE = 0 PPM = 1PPM = 1DTOHx DTHI = 0 DTHI = 1 DTLI = 0 DTLI = 1 DTOLx DTOHx DTHI = 0 DTHI = 1 DTLI = 1 DTLI = 0 DTOLx ī T DTOHx DTHI = 0 DTHI = 1 DTLI = 0 DTLI = 1 DTOLx DTOHx DTHI = 1DTHI = 0DTLI = 1 DTLI = 0 DTOLx 1 L