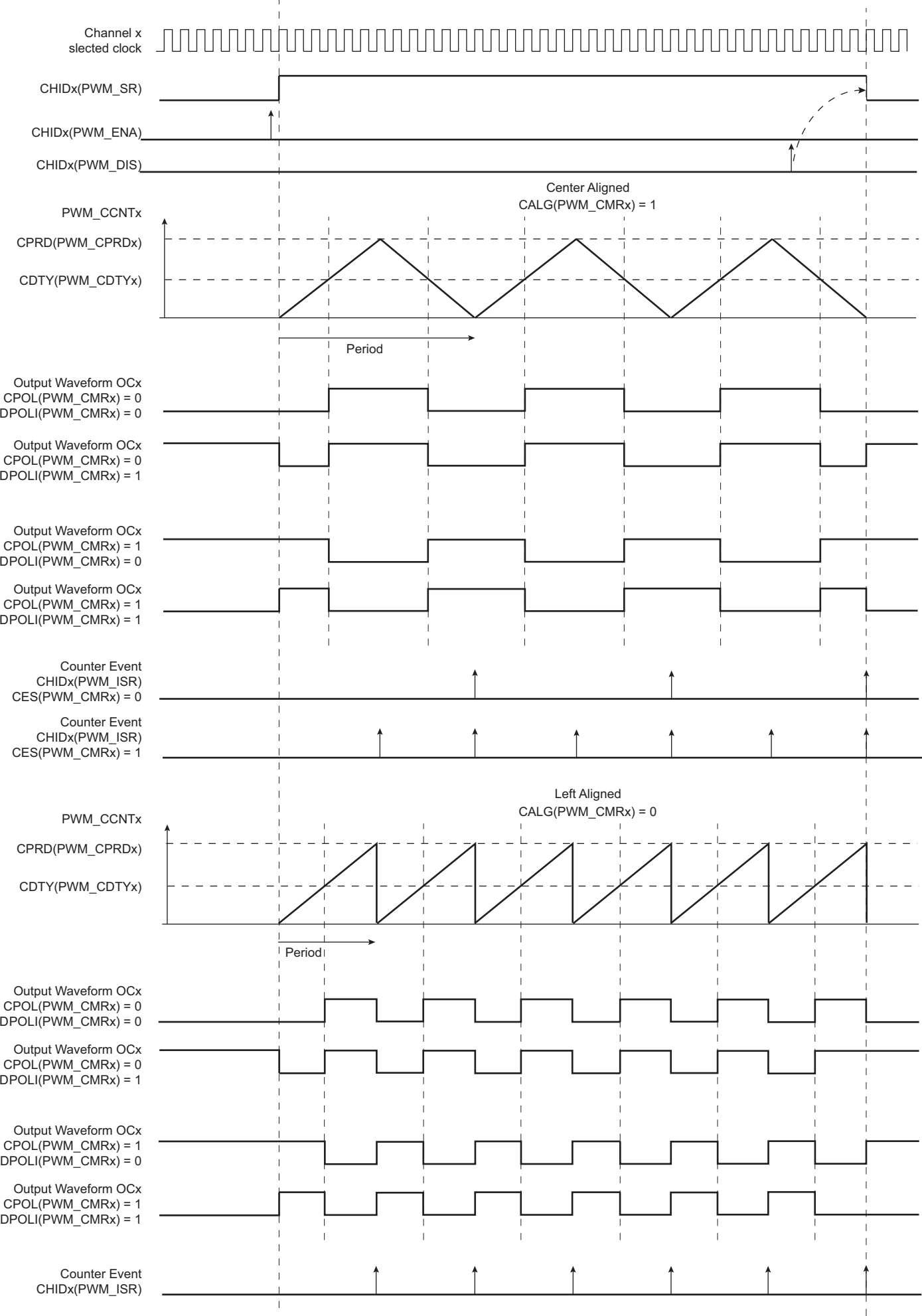
Channel x
slected clock
CHIDx(PWM_SR)
CHIDx(PWM_ENA)
CHIDx(PWM_DIS)
Center Aligned
CALG(PWM_CMRx) = 1
PWM_CCNTx
CPRD(PWM_CPRDx)
CDTY(PWM_CDTYx)
Period
Output Waveform OCx
CPOL(PWM_CMRx) = 0
DPOLI(PWM_CMRx) = 0
Output Waveform OCx
CPOL(PWM_CMRx) = 0
DPOLI(PWM_CMRx) = 1
Output Waveform OCx
CPOL(PWM_CMRx) = 1
DPOLI(PWM_CMRx) = 0
Output Waveform OCx
CPOL(PWM_CMRx) = 1
DPOLI(PWM_CMRx) = 1
Counter Event
CHIDx(PWM_ISR)
CES(PWM_CMRx) = 0
Counter Event
CHIDx(PWM_ISR)
CES(PWM_CMRx) = 1
Left Aligned
CALG(PWM_CMRx) = 0
PWM_CCNTx
CPRD(PWM_CPRDx)
CDTY(PWM_CDTYx)
Period
Output Waveform OCx
CPOL(PWM_CMRx) = 0
DPOLI(PWM_CMRx) = 0
Output Waveform OCx
CPOL(PWM_CMRx) = 0
DPOLI(PWM_CMRx) = 1
Output Waveform OCx
CPOL(PWM_CMRx) = 1
DPOLI(PWM_CMRx) = 0
Output Waveform OCx
CPOL(PWM_CMRx) = 1
DPOLI(PWM_CMRx) = 1
Counter Event
CHIDx(PWM_ISR)