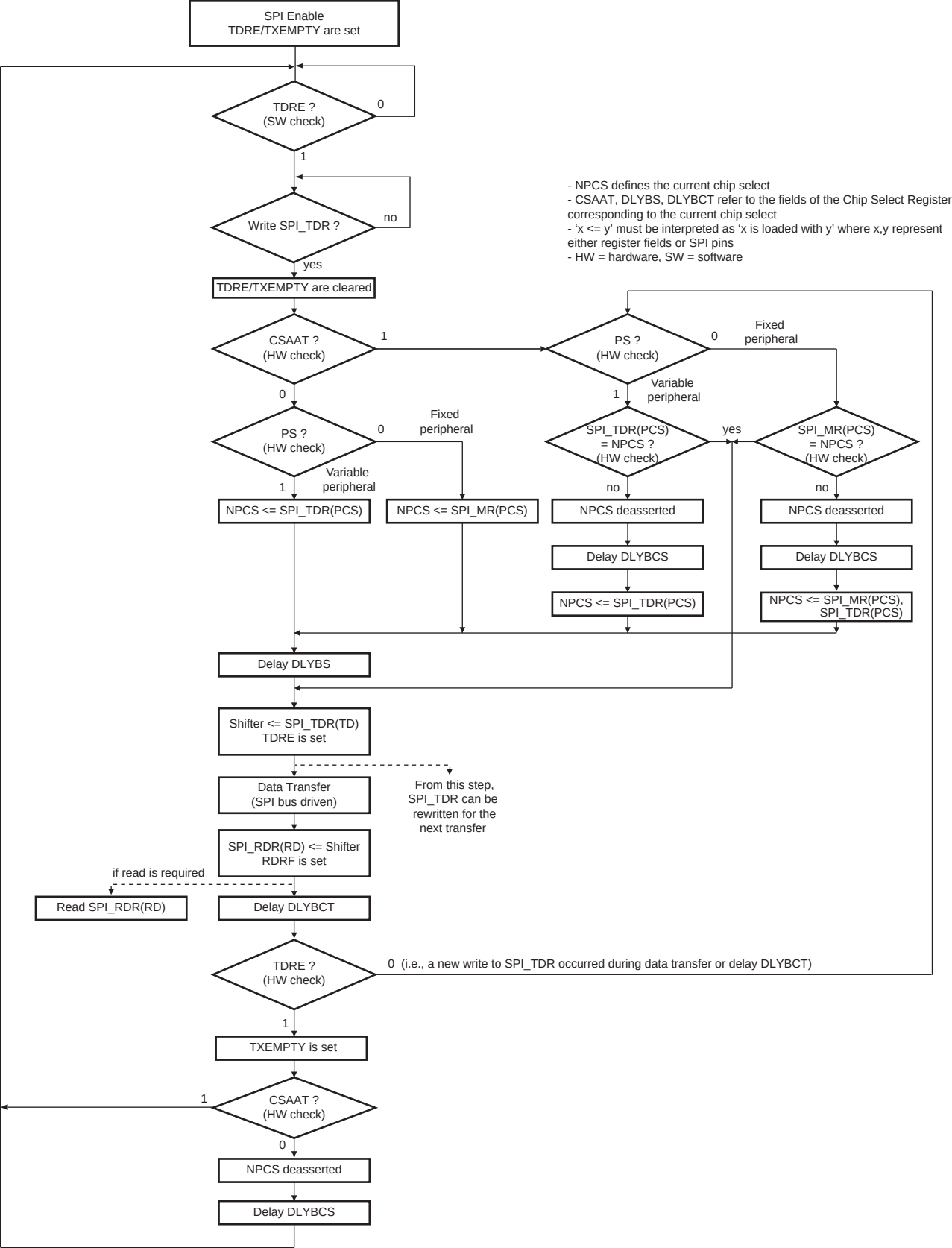
SPI Enable
TDRE/TXEMPTY are set
TDRE ?
(SW check)
0
1
Write SPI_TDR ?
no
yes
TDRE/TXEMPTY are cleared
CSAAT ?
(HW check)
1
0
PS ?
(HW check)
0
Fixed
peripheral
1
Variable
peripheral
SPI_TDR(PCS)
= NPCS ?
(HW check)
yes
SPI_MR(PCS)
= NPCS ?
(HW check)
no
no
NPCS <= SPI_TDR(PCS)
NPCS <= SPI_MR(PCS)
NPCS deasserted
NPCS deasserted
Delay DLYBCS
Delay DLYBCS
NPCS <= SPI_TDR(PCS)
NPCS <= SPI_MR(PCS),
SPI_TDR(PCS)
Delay DLYBS
Shifter <= SPI_TDR(TD)
TDRE is set
Data Transfer
(SPI bus driven)
From this step,
SPI_TDR can be
rewritten for the
next transfer
SPI_RDR(RD) <= Shifter
RDRF is set
if read is required
Read SPI_RDR(RD)
Delay DLYBCT
TDRE ?
(HW check)
0 (i.e., a new write to SPI_TDR occurred during data transfer or delay DLYBCT)
1
TXEMPTY is set
CSAAT ?
(HW check)
1
0
NPCS deasserted
Delay DLYBCS
- NPCS defines the current chip select
- CSAAT, DLYBS, DLYBCT refer to the fields of the Chip Select Register corresponding to the current chip select
- 'x <= y' must be interpreted as 'x is loaded with y' where x,y represent either register fields or SPI pins
- HW = hardware, SW = software