

Bit	7	6	5	4	3	2	1	0	
	TIMEBASE[6:0]								
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	1	

Bits 6:0 – TIMEBASE[6:0] Timebase

This bit field controls the maximum value of a counter that counts CLK_PER cycles to achieve a time interval equal to or larger than 1 μ s. It should be written with one less than the number of CLK_PER cycles that are equal to or larger than 1 μ s. This is used for internal timing of the warmup and settling times.