BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		_	BANK 63
1C00h		1C80h		1D00h		1D80h		1E00h		1E80h		1F00h		1F80h	
	Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers
1C0Bh		1C8Bh		1D0Bh		1D8Bh		1E0Bh		1E8Bh		1F0Bh		1F8Bh	
1C0Ch		1C8Ch		1D0Ch		1D8Ch		1E0Ch	UMTOAP	1E8Ch		1F0Ch		1F8Ch	
								1E0Dh 1E0Eh	UMTOAL UMTOAH						
								1E0Fh							
															Unimplemented Read as '0'
											See Table 2 for				
	Unimplemented Read as '0'		Unimplemented		Unimplemented		Unimplemented				register mapping		See Table 3 for register mapping		
			Read as '0'		Read as '0'		Read as '0'		Unimplemented		details		details		
									Read as '0'						
														1FE3h	
														1FE4h 1FE5h	STATUS_SHAD WREG_SHAD
														1FE6h	BSR_SHAD
														1FE7h 1FE8h	PCLATH_SHAD
														1FE9h	FSROL_SHAD FSROH_SHAD
														1FEAh	FSR1L_SHAD
														1FEBh 1FECh	FSR1H_SHAD —
														1FEDh	STKPTR
1C6Fh		1CEFh		1D6Fh		1DEFh		1E6Fh		1EEFh		1F6Fh		1FEEh 1FEFh	TOSL TOSH
1C70h	Common RAM	1CF0h	Common RAM	1D70h	Common RAM	1DF0h	Common RAM	1E70h	Common RAM	1EF0h	Common RAM	1F70h	Common RAM	1FF0h	Common RAM
1C7Fh	(Accesses 70h-7Fh)	1CFFh	(Accesses 70h-7Fh)	1D7Fh	(Accesses 70h-7Fh)	1DFFh	(Accesses 70h-7Fh)	1E7Fh	(Accesses 70h-7Fh)	1EFFh	(Accesses 70h-7Fh)	1F7Fh	(Accesses 70h-7Fh)	1FFFh	(Accesses 70h-7Fh)
10/11/	7011 71111	101111	7011 71111	10/11/1	7011 71111	121111	7011 71111	15/111	7011 71111]	7011 71111	1 /. !!	7011 7111)	1	7011 7111)
	Legend:	nented da	ta memory locations	read as 'C) '										