

J16

5V MAIN

MP1

DISP_NIRST

D8

3

MIPI_ENABLE PB18

DISP_NIRST

R210 0R

R212 0R

R214 0R

C002

C003

MIPI_TWCK_PC6

MIPI_IRQ_PB16

MIPI_PWM_PB14

MIPI

Mismatched Net Lengths (Tolerance = 0.2mm)

MIPI_D3_P

MIPI_D3_N

MIPI_D2_P

MIPI_D2_N

MIPI_OK_P

MIPI_OK_N

MIPI_D1_P

MIPI_D1_N

MIPI_D0_P

MIPI_D0_N

34 pin FFC/FFPC

GND

100Ω ± 50K differential trace impedance
Routing top or bottom

[illegible]

Pin 1 to 40 connection diagram for the RPi 4B. The diagram shows a 40-pin header with pins numbered 1 to 40. Pins 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, and 40 are connected to GND. Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, and 39 are connected to 3V3. Pins 3, 7, 11, 15, 19, 23, 27, 31, 35, 39, and 40 are connected to 5V MAIN. The diagram also shows connections for various RPi components: RPi TWD PC7 (pin 1), RPi TWICC PC6 (pin 2), RPi GLCCLK PB1 (pin 3), RPi GLCCLK PB1 (pin 4), RPi GLCCLK PB1 (pin 5), RPi GLCCLK PB1 (pin 6), RPi GLCCLK PB1 (pin 7), RPi GLCCLK PB1 (pin 8), RPi GLCCLK PB1 (pin 9), RPi GLCCLK PB1 (pin 10), RPi GLCCLK PB1 (pin 11), RPi GLCCLK PB1 (pin 12), RPi GLCCLK PB1 (pin 13), RPi GLCCLK PB1 (pin 14), RPi GLCCLK PB1 (pin 15), RPi GLCCLK PB1 (pin 16), RPi GLCCLK PB1 (pin 17), RPi GLCCLK PB1 (pin 18), RPi GLCCLK PB1 (pin 19), RPi GLCCLK PB1 (pin 20), RPi GLCCLK PB1 (pin 21), RPi GLCCLK PB1 (pin 22), RPi GLCCLK PB1 (pin 23), RPi GLCCLK PB1 (pin 24), RPi GLCCLK PB1 (pin 25), RPi GLCCLK PB1 (pin 26), RPi GLCCLK PB1 (pin 27), RPi GLCCLK PB1 (pin 28), RPi GLCCLK PB1 (pin 29), RPi GLCCLK PB1 (pin 30), RPi GLCCLK PB1 (pin 31), RPi GLCCLK PB1 (pin 32), RPi GLCCLK PB1 (pin 33), RPi GLCCLK PB1 (pin 34), RPi GLCCLK PB1 (pin 35), RPi GLCCLK PB1 (pin 36), RPi GLCCLK PB1 (pin 37), RPi GLCCLK PB1 (pin 38), RPi GLCCLK PB1 (pin 39), RPi GLCCLK PB1 (pin 40).

