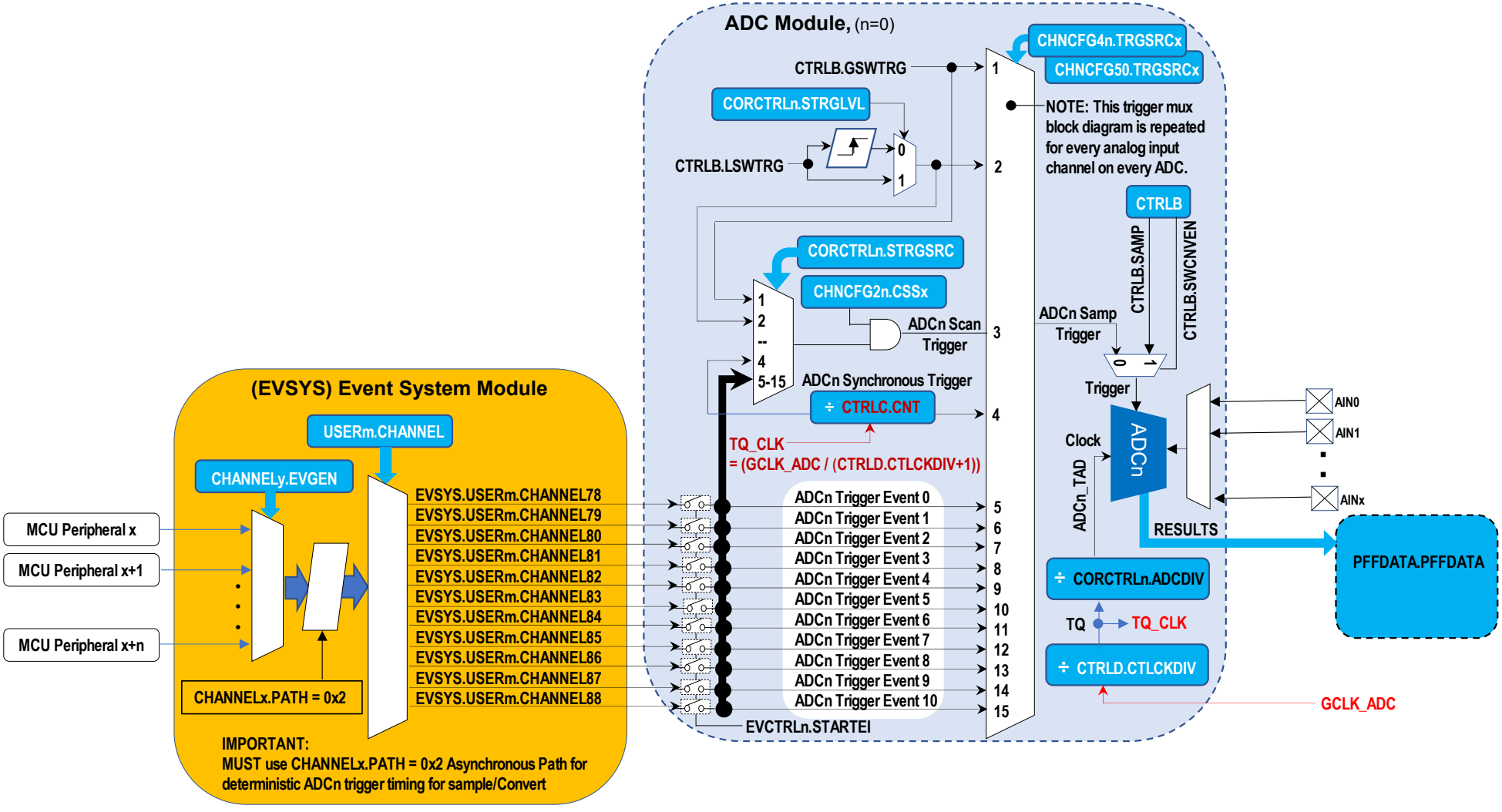
ADC Module, (n=0)
CHNCFG4n.TRGSRCx
CHNCFG50.TRGSRCx
CTRLB.GSWTRG
CORCTRLn.STRGLVL
CTRLB.LSWTRG
NOTE: This trigger mux block diagram is repeated for every analog input channel on every ADC.
CTRLB
CTRLB.SAMP
CTRLB.SWCNVEN
CORCTRLn.STRGSRC
CHNCFG2n.CSSx
ADCn Scan Trigger
ADCn Samp Trigger
ADCn Synchronous Trigger
÷ CTRLC.CNT
Trigger
Clock
ADCn
ADCn_TAD
AIN0
AIN1
AINx
RESULTS
PFFDATA.PFFDATA
TQ_CLK
= (GCLK_ADC / (CTRLD.CTLCKDIV+1))
ADCn Trigger Event 0
ADCn Trigger Event 1
ADCn Trigger Event 2
ADCn Trigger Event 3
ADCn Trigger Event 4
ADCn Trigger Event 5
ADCn Trigger Event 6
ADCn Trigger Event 7
ADCn Trigger Event 8
ADCn Trigger Event 9
ADCn Trigger Event 10
÷ CORCTRLn.ADCDIV
TQ
TQ_CLK
÷ CTRLD.CTLCKDIV
GCLK_ADC
EVCTRLn.STARTEI
(EVSYS) Event System Module
USERm.CHANNEL
CHANNELy.EVGEN
MCU Peripheral x
MCU Peripheral x+1
MCU Peripheral x+n
CHANNELx.PATH = 0x2
EVSYS.USERm.CHANNEL78
EVSYS.USERm.CHANNEL79
EVSYS.USERm.CHANNEL80
EVSYS.USERm.CHANNEL81
EVSYS.USERm.CHANNEL82
EVSYS.USERm.CHANNEL83
EVSYS.USERm.CHANNEL84
EVSYS.USERm.CHANNEL85
EVSYS.USERm.CHANNEL86
EVSYS.USERm.CHANNEL87
EVSYS.USERm.CHANNEL88
IMPORTANT:
MUST use CHANNELx.PATH = 0x2 Asynchronous Path for deterministic ADCn trigger timing for sample/Convert