

BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63	
1C00h	Core Registers	1C80h	Core Registers	1D00h	Core Registers	1D80h	Core Registers	1E00h	Core Registers	1E80h	Core Registers	1F00h	Core Registers	1F80h	Core Registers
1C0Bh		1C8Bh	NVMADRL	1D0Ch	ADLTHL	1D8Bh	RA0PPS	1E0Bh		1E8Bh		1F0Bh	UMTOAP	1F8Bh	
1C0Ch		1C8Ch	NVMADRH	1D0Dh	ADLTHH	1D8Dh	RA1PPS	1E0Ch		1E8Ch		1F0Ch	UMTOAL	1F8Ch	
		1C8Dh	NVMADTL	1D0Eh	ADUTHL	1D8Eh	RA2PPS					1F0Dh	UMTOAH		
		1C8Eh	NVMADTH	1D0Fh	ADUTHH	1D8Fh	RA3PPS					1F0Eh			
		1C8Fh	NVMCON1	1D10h	ADERRL	1D90h	RA4PPS					1F0Fh			
		1C90h	NVMCON2	1D11h	ADERRH	1D91h	RA5PPS								
		1C91h	SCANCON0	1D12h	ADSTPTL	1D92h	RA6PPS								
		1C92h	SCANCON1	1D13h	ADSTPTH	1D93h	RA7PPS								
		1C93h	SCANLADR1	1D14h	ADFLTRL	1D94h	RB0PPS								
		1C94h	SCANLADR2	1D15h	ADFLTRH	1D95h	RB1PPS								
		1C95h	—	1D16h	ADACCL	1D96h	RB2PPS								
		1C96h	SCANHADR1	1D17h	ADACCH	1D97h	RB3PPS								
		1C97h	SCANHADR2	1D18h	ADACCU	1D98h	RB4PPS								
		1C98h	—	1D19h	ADCNTR	1D99h	RB5PPS								
		1C99h	SCANDPS	1D1Ah	ADRPT	1D9Ah	RB6PPS								
		1C9Ah	SCANTRIG	1D1Bh	ADPREVL	1D9Bh	RB7PPS								
		1C9Bh	—	1D1Ch	ADPREVH	1D9Ch	RC0PPS								
		1C9Ch	—	1D1Dh	ADRESL	1D9Dh	RC1PPS								
		1C9Dh	CRCDATA1	1D1Eh	ADRESH	1D9Eh	RC2PPS								
		1C9Eh	CRCDATAH	1D1Fh	ADPCH	1D9Fh	RC3PPS								
		1C9Fh	CRCDATAU	1D20h	—	1DA0h	RC4PPS								
		1CA0h	CRCDATAT	1D21h	ADACQL	1DA1h	RC5PPS								
		1CA1h	CRCOUNTL	1D22h	ADACQH	1DA2h	RC6PPS								
		1CA2h	CRCOUNTH	1D23h	ADCAP	1DA3h	RC7PPS								
		1CA3h	CRCOUNTU	1D24h	ADPREL	1DA4h	RD0PPS <sup>[1]</sup>								
		1CA4h	CRCOUNTT	1D25h	ADPREH	1DA5h	RD1PPS <sup>[1]</sup>								
		1CA5h	CRCCONO	1D26h	ADCON0	1DA6h	RD2PPS <sup>[1]</sup>								
		1CA6h	CRCCON1	1D27h	ADCON1	1DA7h	RD3PPS <sup>[1]</sup>								
		1CA7h	CRCCON2	1D28h	ADCON2	1DA8h	RD4PPS <sup>[1]</sup>								
		1CA8h		1D29h	ADCON3	1DA9h	RD5PPS <sup>[1]</sup>								
				1D2Ah	ADSTAT	1DAAh	RD6PPS <sup>[1]</sup>								
				1D2Bh	ADREF	1DABh	RD7PPS <sup>[1]</sup>								
				1D2Ch	ADACT	1DACH	RE0PPS								
				1DCDh	ADCLK	1DADh	RE1PPS								
				1D2Eh	ADCG1A	1DAEh	RE2PPS								
				1D2Fh	ADCG1B	1DAFh	Unimplemented Read as '0'								
				1D30h	ADCG1C	1DCFh									
				1D31h	ADCG1D <sup>[1]</sup>	1DD0h	TRISC0PPS								
				1D32h	ADCG1E	1DD1h	TRISC1PPS								
				1D33h		1DD2h	TRISC2PPS								
						1DD3h	TRISC3PPS								
						1DD4h	TRISC4PPS								
						1DD5h	TRISC5PPS								
						1DD6h	TRISC6PPS								
						1DD7h	Unimplemented Read as '0'								
1C6Fh		1CEFh		1D6Fh		1DEFh		1E6Fh		1EEFh		1F6Fh			
1C70h	Common RAM (Accesses 70h-7Fh)	1CF0h	Common RAM (Accesses 70h-7Fh)	1D70h	Common RAM (Accesses 70h-7Fh)	1DF0h	Common RAM (Accesses 70h-7Fh)	1E70h	Common RAM (Accesses 70h-7Fh)	1E7Fh	Common RAM (Accesses 70h-7Fh)	1E8Fh	Common RAM (Accesses 70h-7Fh)	1F70h	Common RAM (Accesses 70h-7Fh)
1C7Fh		1CF0h		1D7Fh		1DFFh		1E7Fh		1EFFh		1F7Fh		1FFFh	

Note: 1. Available on 40/44-pin devices only

Legend:

Unimplemented data memory locations, read as '0'

Unimplemented  
Read as '0'

STATUS\_SHAD  
WREG\_SHAD  
BSR\_SHAD  
PCLATH\_SHAD  
FSROL\_SHAD  
FSROH\_SHAD  
FSR1L\_SHAD  
FSR1H\_SHAD  
—  
STKPTR  
TOSL  
TOSH  
Common RAM  
(Accesses  
70h-7Fh)