

```

flx0: flexcom@f801c000 {
    compatible = "atmel,sama5d2-flexcom";
    reg = <0xf801c000 0x200>;
    clocks = <&pmc PMC_TYPE_PERIPHERAL 5>;
    #address-cells = <1>;
    #size-cells = <1>;
    ranges = <0x0 0xf801c000 0x800>;
    status = "disabled";

    uart0: serial@200 {
        compatible = "microchip,sam9x60-usart", "atmel,at91sam9260-usart";
        reg = <0x200 0x200>;
        interrupts = <5 IRQ_TYPE_LEVEL_HIGH 7>;
        dmas = <&dma0
            (AT91_XDMAC_DT_MEM_IF(0) |
             AT91_XDMAC_DT_PER_IF(1) |
             AT91_XDMAC_DT_PERID(0))>,
            <&dma0
            (AT91_XDMAC_DT_MEM_IF(0) |
             AT91_XDMAC_DT_PER_IF(1) |
             AT91_XDMAC_DT_PERID(1))>;
        dma-names = "tx", "rx";
        clocks = <&pmc PMC_TYPE_PERIPHERAL 5>;
        clock-names = "usart";
        atmel,use-dma-rx;
        atmel,use-dma-tx;
        atmel,fifo-size = <16>;
        status = "disabled";
    };
};

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spi0: spi@400 {
    compatible = "microchip,sam9x60-spi", "atmel,at91rm9200-spi";
    reg = <0x400 0x200>;
    interrupts = <5 IRQ_TYPE_LEVEL_HIGH 7>;
    clocks = <&pmc PMC_TYPE_PERIPHERAL 5>;
    clock-names = "spi_clk";
    dmas = <&dma0
        (AT91_XDMAC_DT_MEM_IF(0) |
         AT91_XDMAC_DT_PER_IF(1) |
         AT91_XDMAC_DT_PERID(0))>,
        <&dma0
        (AT91_XDMAC_DT_MEM_IF(0) |
         AT91_XDMAC_DT_PER_IF(1) |
         AT91_XDMAC_DT_PERID(1))>;
    dma-names = "tx", "rx";
    atmel,fifo-size = <16>;
    status = "disabled";
};

i2c0: i2c@600 {
    compatible = "microchip,sam9x60-i2c";
    reg = <0x600 0x200>;
    interrupts = <5 IRQ_TYPE_LEVEL_HIGH 7>;
    #address-cells = <1>;
    #size-cells = <0>;
    clocks = <&pmc PMC_TYPE_PERIPHERAL 5>;
    dmas = <&dma0
        (AT91_XDMAC_DT_MEM_IF(0) |
         AT91_XDMAC_DT_PER_IF(1) |
         AT91_XDMAC_DT_PERID(0))>,
        <&dma0
        (AT91_XDMAC_DT_MEM_IF(0) |
         AT91_XDMAC_DT_PER_IF(1) |
         AT91_XDMAC_DT_PERID(1))>;
    dma-names = "tx", "rx";
    atmel,fifo-size = <16>;
    status = "disabled";
};
};

```