BANK 61

1E80h 1E8Bh	Core registers
1E8Ch	ANSELA
1E8Dh	WPUA
1E8Eh	ODCONA
1E8Fh	SLRCONA
1E90h	INLVLA
1E91h	IOCAP
1E92h	IOCAN
1E93h	IOCAF
1E94h 1E9Fh	Unimplemented Read as '0'
1EA0h	ANSELC(1)
1EA1h	WPUC(1)
1EA2h	ODCONC(1)
1EA3h	SLRCONC(1)
1EA4h	INLVLC(1)
1EA5h	IOCCP(1)
1EA6h	IOCCN(1)
1EA7h	IOCCF(1)
1EA8h 1EE0h	Unimplemented Read as '0'
1EE1h	RA1I2C(2)
1EE2h	RA2I2C(2)
1EE3h 1EE8h	Unimplemented Read as '0'
1EE9h	RC0I2C(1)
1EEAh	RC1I2C(1)
1EEBh	—
1EECh	—
1EEDh	—
1EEEh	—
1EEFh	—
1EF0h 1EFFh	Common RAM (Accesses 70h-7Fh)

Note:
1. 14/16-pin devices only
2. 8-pin devices only

Legend:

Unimplemented data memory locations, read as '0'