BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		_	BANK 29		BANK 30		BANK 31	
C00h		C80h		D00h		D80h		E00h		E80h		F00h		F80h		
	Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers	
COBh		C8Bh		D0Bh		D8Bh		EOBh		E8Bh		F0Bh		F8Bh		
C0Ch	_	C8Ch	_	D0Ch		D8Ch		E0Ch		E8Ch		F0Ch		F8Ch		
C0Dh	_		_													
C0Eh	_		_													
C0Fh C10h		ŀ														
C10h	<u> </u>	ŀ	<u> </u>													
C1111	_	ŀ	_													
C12h	_	ŀ	_													
C14h	_	ŀ	_													
C15h	_	ľ	_													
C16h	_	ļ	_													
C17h	_	Ī	_													
C18h	_		_													
C19h	_		_													
C1Ah	_		_		Unimplemented		Unimplemented		Unimplemented		Unimplemented		Unimplemented		Unimplemented	
C1Bh					Read as '0'		Read as '0'		Read as '0'		Read as '0'		Read as '0'		Read as '0'	
C1Ch	_		_													
C1Dh	_	-	_													
C1Eh C1Fh	<u> </u>	C9Fh														
C20h	_	CA0h														
CZUII		CAUII														
	Unimplemented		Unimplemented													
	Read as '0'		Read as '0'													
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh		
C70h	Common RAM	CF0h	Common RAM	D70h	Common RAM	DF0h	Common RAM	E70h	Common RAM	EF0h	Common RAM	F70h	Common RAM	FF0h	Common RAM	
6751	(Accesses	CEEL	(Accesses	5751	(Accesses	D.E.E.	(Accesses	F7F'	(Accesses		(Accesses		(Accesses		(Accesses	
C7Fh	70h-7Fh)	CFFh	70h-7Fh)	D7Fh	70h-7Fh)	DFFh	70h-7Fh)	E7Fh	70h-7Fh)	EFFh	70h-7Fh)	F7Fh	70h-7Fh)	FFFh	70h-7Fh)	
1	Logond:															
	Legend:				01											

Legend:
Unimplemented data memory locations, read as '0'