Address	Device	
	PIC18F45Q10	PIC18F26Q10 PIC18F46Q10

Note 1	Stack (31 Levels)

00 0000h	Reset Vector	
…	…	
00 0008h	Interrupt Vector High	
…	…	
00 0018h	Interrupt Vector Low	
…	…	
00 001Ah 00 7FFFh	Program Flash Memory (16 KW)	Program Flash Memory (32 KW)
00 8000h 00 FFFFh	Not Present(2)	
01 0000h 01 FFFFh		Not Present(2)
02 0000h 1F FFFFh		
20 0000h 20 00FFh	User IDs (128 Words)(3)	
20 0100h 2F FFFFh	Reserved	
30 0000h 30 000Bh	Configuration Words (6 Words)(3)	
30 000Ch 30 02FFh	Reserved	
30 0300h 30 FFFBh	Unimplemented	
31 0000h 31 00FFh	Data EEPROM (256 Bytes)	Data EEPROM (1 k Bytes)
31 0100h 31 03FFh	Unimplemented	
31 0400h 3F FFFBh		Unimplemented
3F FFFCh 3F FFFDh	Revision ID (1 Word)(4)	
3F FFFEh 3F FFFFh	Device ID (1 Word)(4)	

Note 1: The stack is a separate SRAM panel, apart from all user memory panels.

2: The addresses do not roll over. The region is read as ‘0’.

3: Not code-protected.

4: Device/Revision IDs are hard-coded in silicon.