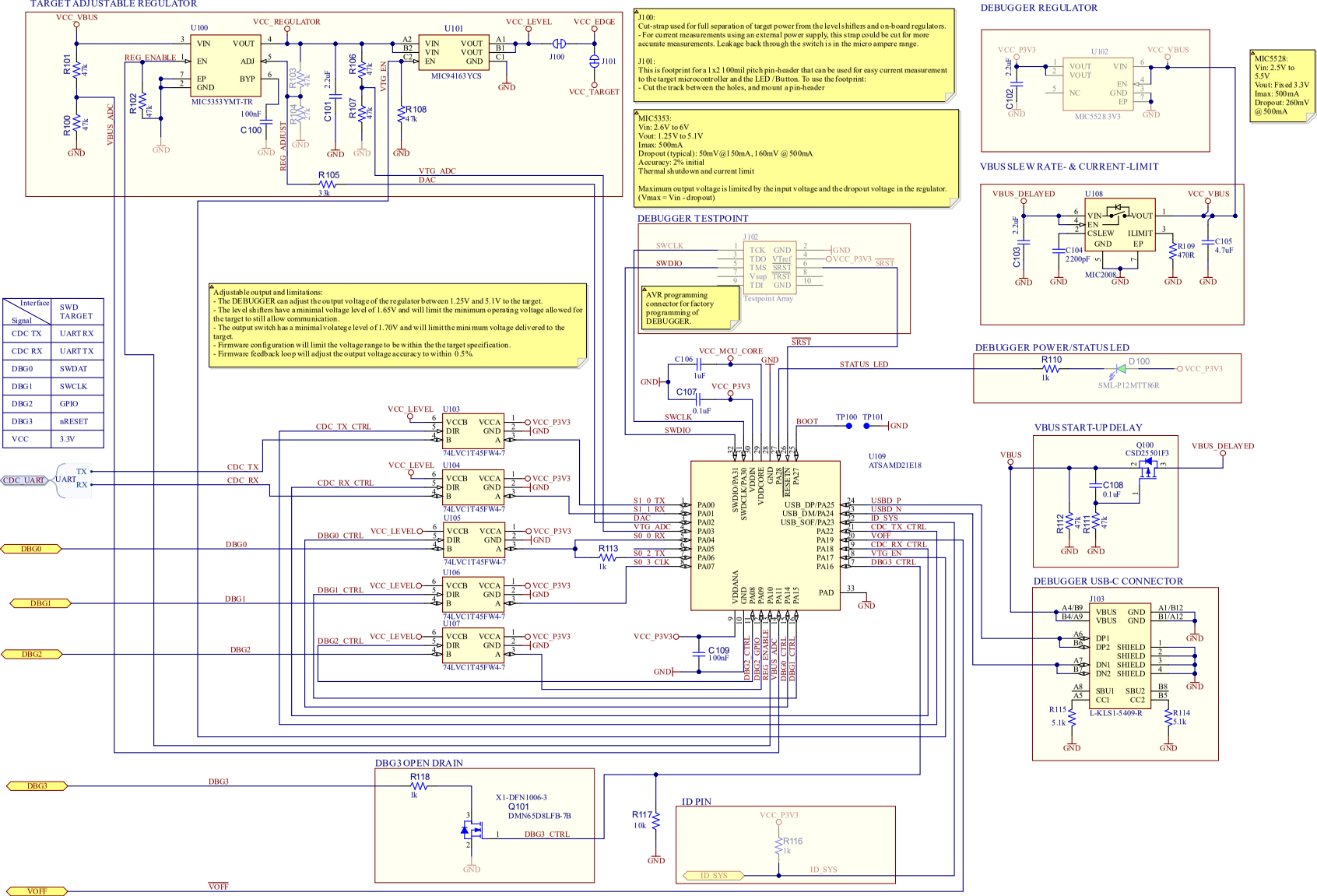
TARGET ADJUSTABLE REGULATOR
U100
MIC5353YMT-TR
U101
MIC94163YCS
VCC_VBUS
VCC_REGULATOR
VCC_LEVEL
VCC_EDGE
VCC_TARGET
REG_ENABLE
VTG_EN
VBUS_ADC
REG_ADJUST
VTG_ADC
DAC
J100
J101
R101 47k
R100 47k
R102 47k
R103 47k
R104 27k
R106 47k
R107 47k
R108 47k
R105 3.3k
C100 100nF
C101 2.2uF
J100:
Cut-strap used for full separation of target power from the level shifters and on-board regulators.
- For current measurements using an external power supply, this strap could be cut for more accurate measurements. Leakage back through the switch is in the micro ampere range.
J101:
This is footprint for a 1x2 100mil pitch pin-header that can be used for easy current measurement to the target microcontroller and the LED / Button. To use the footprint:
- Cut the track between the holes, and mount a pin-header
MIC5353:
Vin: 2.6V to 6V
Vout: 1.25V to 5.1V
Imax: 500mA
Dropout (typical): 50mV@150mA, 160mV @500mA
Accuracy: 2% initial
Thermal shutdown and current limit
Maximum output voltage is limited by the input voltage and the dropout voltage in the regulator.
(Vmax = Vin - dropout)
DEBUGGER REGULATOR
U102
MIC5528 3V3
VCC_P3V3
VCC_VBUS
C102 2.2uF
MIC5528:
Vin: 2.5V to 5.5V
Vout: Fixed 3.3V
Imax: 500mA
Dropout: 260mV @500mA
VBUS SLEW RATE- & CURRENT-LIMIT
U108
MIC2008
VBUS_DELAYED
VCC_VBUS
C103 2.2uF
C104 2200pF
R109 470R
C105 4.7uF
DEBUGGER TESTPOINT
J102
Testpoint Array
SWCLK
SWDIO
SRST
AVR programming connector for factory programming of DEBUGGER.
Adjustable output and limitations:
- The DEBUGGER can adjust the output voltage of the regulator between 1.25V and 5.1V to the target.
- The level shifters have a minimal voltage level of 1.65V and will limit the minimum operating voltage allowed for the target to still allow communication.
- The output switch has a minimal volatege level of 1.70V and will limit the minimum voltage delivered to the target.
- Firmware configuration will limit the voltage range to be within the the target specification.
- Firmware feedback loop will adjust the output voltage accuracy to within 0.5%.
Interface / Signal: SWD TARGET
CDC TX: UART RX
CDC RX: UART TX
DBG0: SWDAT
DBG1: SWCLK
DBG2: GPIO
DBG3: nRESET
VCC: 3.3V
C106 1uF
C107 0.1uF
VCC_MCU_CORE
VCC_P3V3
STATUS_LED
DEBUGGER POWER/STATUS LED
R110 1k
D100
SML-P12MTT86R
BOOT
TP100
TP101
U109
ATSAMD21E18
VBUS START-UP DELAY
Q100
CSD25501F3
VBUS
VBUS_DELAYED
C108 0.1uF
R112 47k
R111 47k
DEBUGGER USB-C CONNECTOR
J103
L-KLS1-5409-R
R115 5.1k
R114 5.1k
U103
U104
U105
U106
U107
74LVC1T45FW4-7
CDC_TX_CTRL
CDC_RX_CTRL
DBG0_CTRL
DBG1_CTRL
DBG2_CTRL
CDC_UART
TX
RX
CDC_TX
CDC_RX
DBG0
DBG1
DBG2
S1_0_TX
S1_1_RX
DAC
VTG_ADC
S0_0_RX
S0_2_TX
S0_3_CLK
R113 1k
USB_DP/PA25
USB_DM/PA24
USB_SOF/PA23
USBD_P
USBD_N
ID_SYS
CDC_TX_CTRL
VOFF
CDC_RX_CTRL
VTG_EN
DBG3_CTRL
C109 100nF
DBG3 OPEN DRAIN
R118 1k
X1-DFN1006-3
Q101
DMN65D8LFB-7B
DBG3
DBG3_CTRL
R117 10k
ID PIN
R116 1k
ID_SYS
VOFF