BANK 61

1E80h	Core Registers
1E8Bh	
1E8Ch	ANSELA
1E8Dh	WPUA
1E8Eh	ODCONA
1E8Fh	SLRCONA
1E90h	INLVLA
1E91h	IOCAP
1E92h	IOCAN
1E93h	IOCAF
1E94h	—
1E95h	—
1E96h	ANSELB(2)
1E97h	WPUB(2)
1E98h	ODCONB(2)
1E99h	SLRCONB(2)
1E9Ah	INLVLB(2)
1E9Bh	IOCBP(2)
1E9Ch	IOCBN(2)
1E9Dh	IOCBF(2)
1E9Eh	—
1E9Fh	—
1EA0h	ANSELC
1EA1h	WPUC
1EA2h	ODCONC

1EA3h	SLRCONC
1EA4h	INLVLC
1EA5h	IOCCP
1EA6h	IOCCN
1EA7h	IOCCF
1EA8h	—
1EA9h	—
1EAAh	—
1EABh	—
1EACh	—
1EADh	—
1EAEh	—
1EAFh	Unimplemented Read as '0'
1EB3h	
1EB4h	—
1EB5h	—
1EB6h	—
1EB7h	—
1EB8h	—
1EB9h	—
1EBAh	—
1EBBh	—
1EBCh	Unimplemented Read as '0'
1ECCh	

1ECDh	IOCWP
1ECEh	IOCWN
1ECFh	IOCWF
1ED0h	Unimplemented Read as '0'
1EE2h	
1EE3h	—
1EE4h	—
1EE5h	RB4I2C(1)
1EE6h	RB5I2C(1)
1EE7h	RB6I2C(1)
1EE8h	RB7I2C(1)
1EE9h	RC0I2C(2)
1EEAh	RC1I2C(2)
1EEBh	—
1EECh	RC4I2C(2)
1EEDh	RC5I2C(2)
1EEEh	—
1EEFh	—
1EF0h	Common RAM (Accesses 70h-7Fh)
1EFFh	

Note: **1. Available on 20-pin devices only**

2. Available on 14-pin devices only

Legend:

Unimplemented data memory locations, read as '0'