SyncE Configuration

Clock Source Nomination and State

Clock Source	Nominated	Port	Priority	SSM Overwrite	Hold Off	ANEG mode	LOCS	SSM	WTR	Clear WTR
1	☑	2	0	Disabled	Disabled	None				none
2	☐	1	0	Disabled	Disabled	None				none
3	☐	S-CLK	0	Disabled	Disabled	None				none

Clock Selection Mode and State

Mode	Source	WTR Time	SSM Hold Over	SSM Free Run	EEC Option	State	Clock Source	LOL	DHOLD
Auto Revertive	1	Disable	Disabled	Disabled	1	Locked	1		

Station Clock Configuration and Clock hardware

Clock input frequency	Clock output frequency	Clock hardware id	Clock F/W version
Disabled	Disabled	ZL 30772	1770

Save Reset

SyncE Ports

Port	SSM Enable	Tx SSM	Rx SSM	1000BaseT Mode
*	☑			
1	☑	QL LINK	QL LINK	Slave
2	☑	QL DNU	QL PRC	Slave
3	☐			Slave
4	☑	QL PRC	QL DNU	Master
5	☐			Slave
6	☑	QL LINK	QL LINK	Slave
7	☑	QL LINK	QL LINK	Slave
8	☐			Slave

PTP Ports (8265.1)

Instance	Rx SSM	PTSF
1	QL NONE	None
2	QL NONE	None
3	QL NONE	None