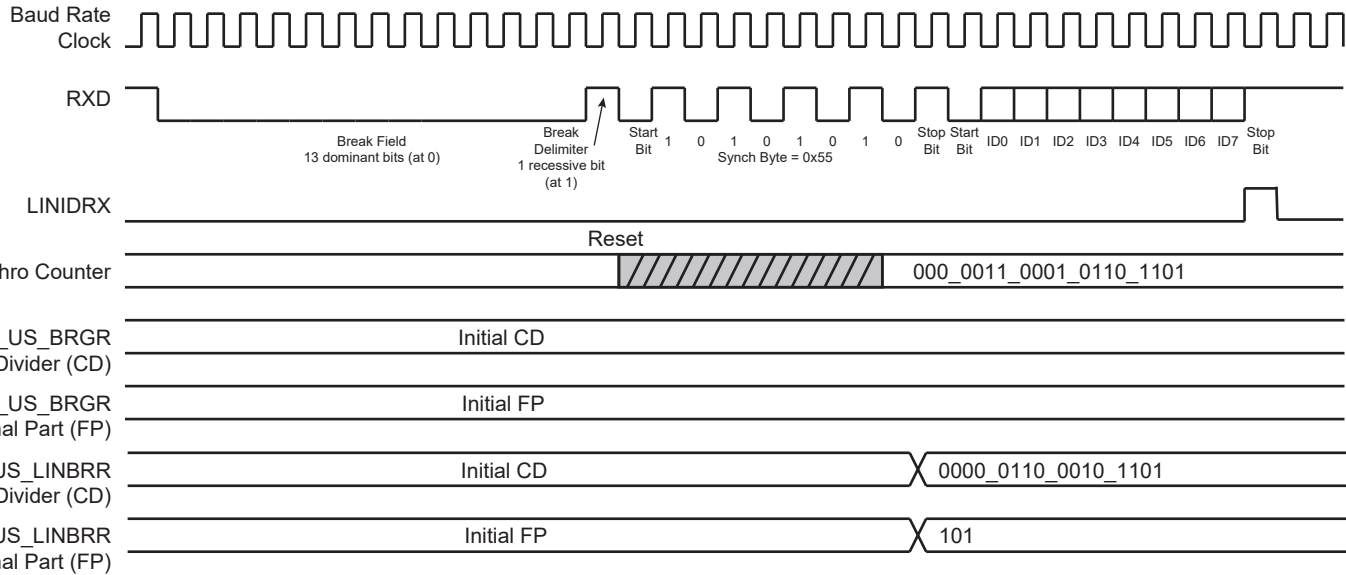
Baud Rate Clock
RXD
Break Field
13 dominant bits (at 0)
Break Delimiter
1 recessive bit
(at 1)
Start Bit
1 0 1 0 1 0 1 0
Synch Byte = 0x55
Stop Bit
Start Bit
ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7
Stop Bit
LINIDRX
Reset
Synchro Counter
000_0011_0001_0110_1101
FLEX_US_BRGR Clock Divider (CD)
Initial CD
FLEX_US_BRGR Fractional Part (FP)
Initial FP
FLEX_US_LINBRR Clock Divider (CD)
Initial CD
0000_0110_0010_1101
FLEX_US_LINBRR Fractional Part (FP)
Initial FP
101